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Power goes digital

DESIGNERS LACK SIMPLE TOOLS TO SQUEEZE PERFORMANCE OUT OF MICROCONTROLLERS IN POWER CONVERTERS. EASY-TO-UNDERSTAND GUIDELINES CAN HELP DESIGNERS TAKE ADVANTAGE OF ANALOG KNOWLEDGE TO EASE THE TRANSITION INTO DIGITAL CONTROL FOR POWER DESIGNS.

Power-design engineers are starting to use digital control in power converters, but the transition has been slow and limited. Many power designers erroneously believe that only high-end systems justify the burden of DSP chips and that simple microcontrollers lack the throughput necessary for reasonable performance in common converters. In reality, the biggest obstacle to technological growth has been that digital and analog designers speak different languages, which hampers communication.

A typical design session for a digitally controlled converter starts with a power engineer sizing the output LC filter based on switching frequency and a firmware engineer writing microcontroller code to adjust the output as a function of measured voltage. After guessing control gains and failing to achieve a fast stable voltage response, the engineer deems the microcontroller inadequate, and a DSP is too expensive and power-hungry for this simple application.

However, engineers cannot completely independently write filter-selection and feedback-control code: They must modify analog-design rules for sizing filters to accommodate processing and update delays in digital controllers, and they must streamline firmware algorithms from motion control to run quickly enough to keep the filter from ringing. Once engineers identify and understand the critical issues, optimization tends to flow naturally.

All engineers understand a scope trace, but few are comfortable going back and forth from time domain to S and Z domains, so the resulting trial-and-error responses tend to be disappointing. Engineers require some simple tools and guidelines from multiple disciplines that they can easily understand and apply.

DESIGN EXAMPLE

The buck converter in **Figure 1** has an inexpensive 8-bit PIC16F818 microcontroller with slow A/D conversion and no hardware multiplier. Using a simple microcontroller illustrates universal digital-power-design concepts, and it's easier to port code to a higher capability device than to do the reverse.

The PIC16F818 has an ADC to measure output voltage and a PWM to adjust the duty cycle of the integrated half-bridge power-stage TDA21201. The output voltage for this synchronous rectifier is the input voltage scaled by the ratio of high time

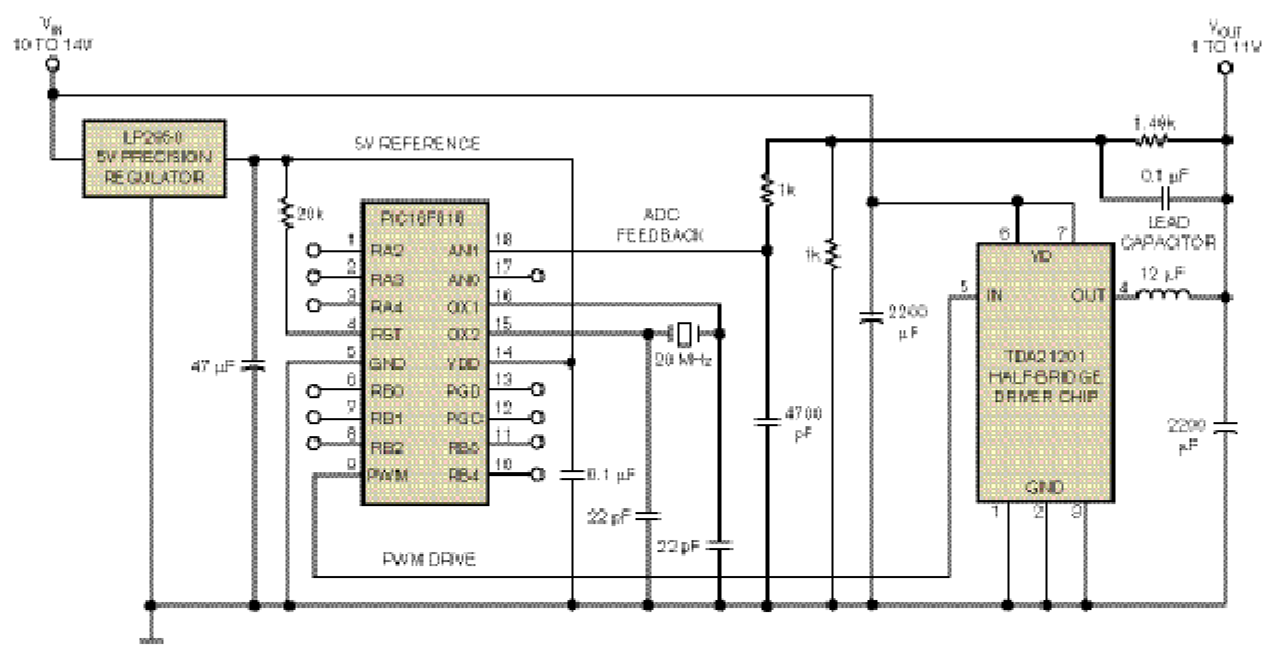

Figure 1 This buck converter has an 8-bit PIC16F818 microcontroller with slow A/D conversion and no hardware multiplier.

to the total switching period, smoothed by the LC filter (**Figure 2**). The control algorithm that calculates PWM drive to obtain the desired ADC voltage is PID (proportional-integral differential). It repeatedly adjusts duty cycle to maintain a fast stable output voltage in response to load and input variations.

The converter is an 80W (1 to $11V_{OUT}$ at 7.3A) nonisolated buck converter, whose total parts cost less than $8 based on distributor prices—hence, the name, "8-buck converter." Key performance parameters include 92% efficiency and 12-mV rms ripple at a 156-kHz switching frequency. The microcontroller has a 20-MHz clock and performs PID-control updates every 25.6 μsec. **Figure 3** illustrates the closed-loop transient response of the converter to a 3A step load, which is comparable with that of common converters with analog-control loops. This example takes the open-loop response at a fixed duty cycle (PID gains at zero) to illustrate how a properly implemented PID loop quickly compensates for voltage droop without ringing.

Although this converter offers the opportunity for firmware customization, designers must accept that digital control adds delays that may impact converter performance. Given the same switching frequency, a converter with a digital-control loop has a lower bandwidth than its analog counterpart, so a larger inductor and capacitor may be necessary in the filter. The converter bandwidth must exceed the resonant frequency of the filter to preclude ringing, so select the LC time constant for controllability.

The effective lag in a digital-control loop is the combination of two effects: processing delay and update interval. Processing delay is the time it takes to convert analog feedback to digital, process the control-algorithm calculations, and then adjust output drive. Update interval is the time between adjustments of output drive. These terms define how often (update interval) the system corrects and how old (processing delay) the information is that the correction used.

Although tools are available to precisely analyze mixed-signal systems, they tend to be somewhat costly and specialized and do not promote an intuitive understanding of critical concepts. To make digital-power control accessible to the most people, this article uses the following analog equivalent based on reasonable approximations. The resultant circuit is simple enough to run on evaluation versions of Spice. Engineers can then take advantage of decades of analog knowledge in the power field to promote greater understanding of digital control.

ANALOG EQUIVALENT

The first step in creating an analog equivalent of a switching converter with digital control is to average the power stage. Averaging is valid because the switching frequency is much higher than the LC-filter resonance. You then perform a similar averaging process with the PID-control algorithm and associated delays. RC networks simulate the processing and update delays. This imprecise approximation is reasonable and effective, and multiple hardware cases validate it.

Figure 4 shows the Spice equivalent of the 8-buck converter in **Figure 1** You can step the I_{LOAD} independent current source or V_{REF} voltage source in the time domain to capture the closed-loop transient response at the V_{OUT} test point.

The 2.4 gain of ESWAVG is the ratio of the nominal 12V input voltage to the 5V range of the PWM command. This example uses measured values for LC components and equivalent series resistances for improved accuracy and increases R_L to approximate switch and pc-board resistance. This scenario added the 0.1-μF lead capacitor in the ADC resistive-divider network after initial simulations indicated it could improve transient performance.

The microcontroller calculates the PID-control loop in firmware every update interval as follows:

- $V_{ERR}=V_{REF}-V_{ADC}$; error=setpoint−measured.
- $V_{ERRDIFF}=V_{ERR}-V_{ERRLAST}$; differential error between samples.
- $V_{ERRLAST}=V_{ERR}$; save current error for next differential calculation.

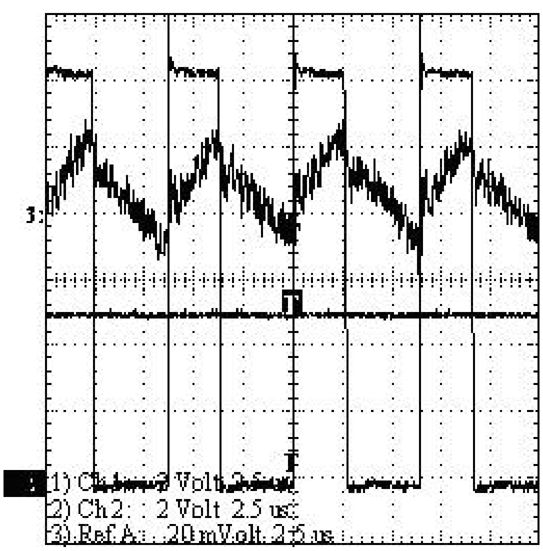

Figure 2 The converter waveforms show that the output voltage is the average of the switching-power-stage values. Waveform 1 is the switching-power stage (2V/div, 2.5 μsec/div). Waveform 2 is the filtered output voltage (2V/div, 2.5 μsec/div). Waveform 3 is the output-voltage ripple (20 mV/div, 2.5 μsec/div).

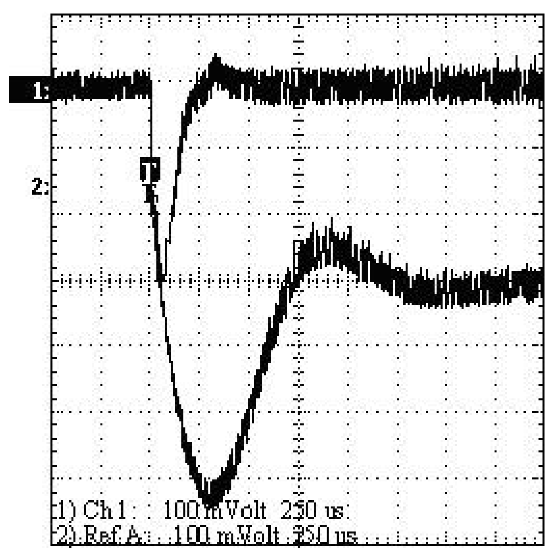

Figure 3 The closed-loop transient response of the converter to a 3A step load compares with that of common converters with analog-control loops.

- $P=K_P\times V_{ERR}$; K_P=proportional gain=4 in 8-buck code.
- $I=I+K_I\times V_{ERR}$; K_I=integral gain=0.25 in 8-buck code.
- $D=K_D\times V_{ERRDIFF}$; K_D=diifferential gain=4 in 8-buck code.
- PWM=PID=P+I+D; make PWM-output adjustment.

PID gain terms K_P, K_P, and K_D are ratios of the most significant bit of PWM to ADC values in microfirmware.

The EPID op amp simulates the PID firmware in the Spice circuit with the following RC components:

- Select R_{IN}=10K.
- $R_{PROP}=K_P\times R_{IN}=4\times 10K=$ 40K.
- $C_{INT}=T_{UPDATE}/(K_I\times R_{IN})=$ 25.6 μsec/(0.25×10K)×0.01 μF.
- $C_{DIFF}=K_D\times T_{UPDATE}/R_{PROP}=$ 4×25.6 μsec 40K×0.0025 μF.

T_{UPDATE} is the 25.6-μsec update interval of the microcontroller, whose associated delay R_{UPDATE} and C_{UPDATE} simulate. The processing delay is the sum of the A/D-conversion time, 19.2 μsec, and the PID-calculation time, 19.2 μsec, rounded up to the next interval of the switching period, 6.4 μsec.

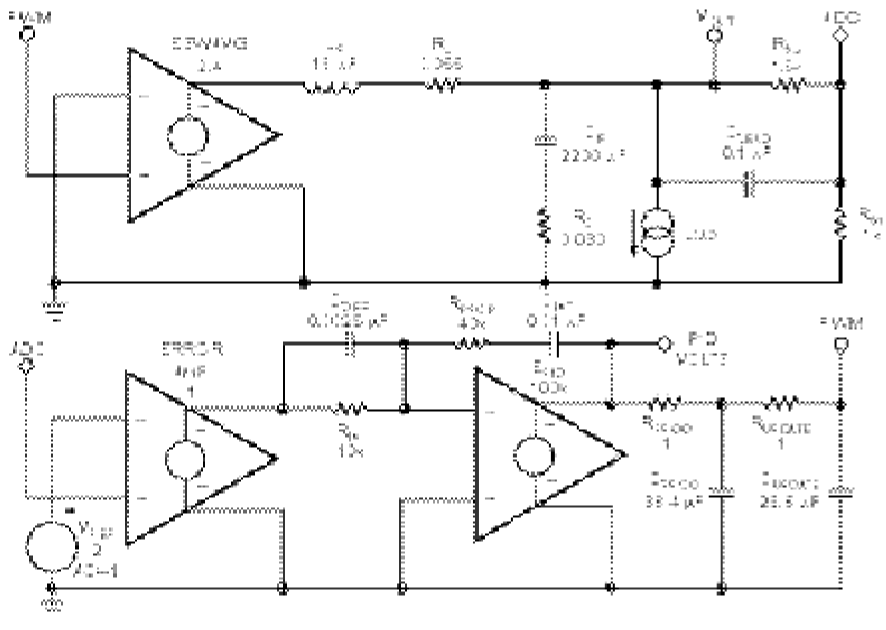

Figure 4 The 8-buck converter of Figure 1 has an analog Spice equivalent.

You measure loop gain and phase margin at the ADC symbol after the power stage by sweeping V_{REF} in the frequency domain. You must first break the feedback loop by removing the ADC symbol from the error amp and connecting V_{REF} to the noninverting input of the error amp with the inverting input grounded. **Figure 5** shows the loop-gain Bode plot, which indicates 2.4-kHz control bandwidth (frequency at unity gain, or 0 dB) with 45° phase margin (phase at unity-gain frequency).

One limitation of the analog model is that it allows greater differential compensation than is possible in digital hardware.

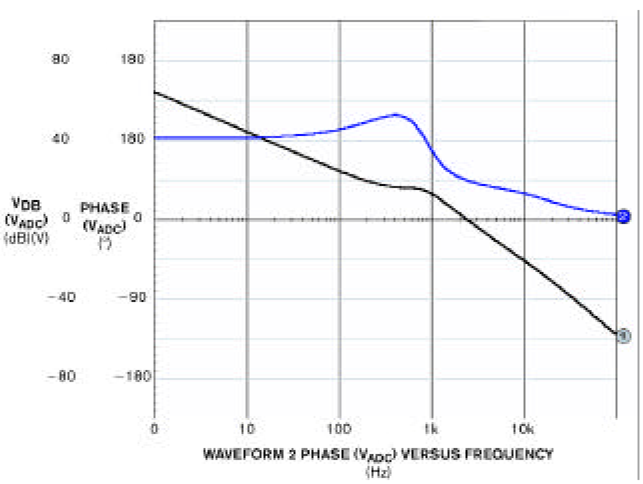

Figure 5 The control-loop gain indicates 2.4-kHz bandwidth and a 45° phase margin.

Phase lead requires a prediction based on the recent past that is invalid with old data, so processing and update delays limit the gain term, K_D. Excessive differential gain appears in hardware as nonlinear ringing, and it decays to a stepped load, in contrast to the sinusoidal ring and exponential decay of a linear system. The simulation determined the lead capacitor in the feedback network of **Figure 1** to compensate for this effect.

In general, the compensator cannot achieve more than 45° lead within the bandwidth of the control loop, so check that the phase at test point PID is less than 225° (inverting loop is initially 180°) at the unity-gain frequency of the entire loop. If the phase exceeds this limit, then accept lower gain and bandwidth or add analog lead to the circuit. The basis of this design guideline comes from the control bandwidth having a direct relationship to the digital delays that limit differential gain.

DESIGN GUIDELINES

The real value of this model is the intuitive understanding that it provides and the ability to take advantage of a designer's knowledge of traditional power converters. For example, rules of thumb say that the control bandwidth must be at least four times lower than the switching frequency. Most loops are closer to a decade below the switching frequency, so 6.3 is a reasonable goal, because it is halfway between 4 and 10 on a log scale. However, anyone who has used a microcontroller to control a power converter finds that this goal is nearly impossible to accomplish. The update interval of the control loop is usually slower than the switching frequency, and you must also consider the additional delays of processing the ADC and PID, which leads to the first two guidelines in the **sidebar**, "Design guidelines for digital-power control."

Once you bound the control bandwidth for a digital converter, you can then approximate the LC resonant frequency because it must be within the control bandwidth. The **sidebar**'s **Guide-**

line 3 assumes that the LC frequency is no more than half the control bandwidth, which is 6.3 times less than the critical frequency. (The 6.3 cancels 2π in the LC equation.) **Guideline 3** is an additional design constraint beyond traditional efforts to limit switching ripple.

PWM resolution alone does not limit the switching frequency of a digital converter. Effective control resolution can be significantly higher than PWM resolution because multiple PWM corrections take place within the time constant of the LC filter. Additionally, effective control resolution can be higher than ADC resolution because you integrate multiple readings, and inherent switching noise acts as averaging dither. However, quantization ripple (sometimes incorrectly referred to as "limit cycling") may occur as the output voltage varies between two neighboring ADC levels (least significant bits), because the filter time constant is usually insufficient to mask oversampling. **Guideline 4** in the **sidebar** covers PWM-frequency selection to balance ripple and resolution.

Despite the precise appearance of these equations, the guidelines are based on approximations that users can adjust. For example, the design exceeded the calculated PWM limit to round up to the nearest power of two, based on the 20-MHz microcontroller clock///OK?///. Some tweaking may occur based on hardware performance, but the guidelines provide a reasonable starting point and strong advantage over trial-and-error approaches.

DESIGN GUIDELINES FOR DIGITAL-POWER CONTROL

GUIDELINE 1: CRITICAL FREQUENCY

$f(critical)=1/[T_{PROCESS}+T_{UPDATE}]=1/[(T_{ADC}+T_{PID})+T_{UPDATE}]$.

In the 8-buck example, $1/[(19.2\ \mu sec+19.2\ \mu sec)+25.6\ \mu sec]$=15.6-kHz limit<<156-kHz switching.

Comment: Digital delays rather than switching frequency limit converter performance.

GUIDELINE 2: CONTROL BANDWIDTH

f(control)<f(critical)/4. (Factor of 4 is the limit, 10 is common, and 6.3 is the goal.)

In the 8-buck example, 15.6 kHz/6.3=2.5 kHz (close to the 2.4-kHz simulation result).

Comment: Critical frequency bounds control-loop bandwidth.

GUIDELINE 3: LC FILTER

$LC^{1/2}>2/f(critical)=2/15.6\ kHz=128\ \mu sec$.

In the 8-buck example, $[12\ \mu H\times 2200\ \mu F]^{1/2}=162\ \mu sec>128\ \mu sec$ (satisfied in design).

Comment: Contain the LC-filter resonance within the loop bandwidth.

GUIDELINE 4: PWM FREQUENCY

$f(PWM)<[f(CLK)/2^{RES(ADC)}]\times[LC^{1/2}/T_{UPDATE}]\times[V_{MEAS}/V_{IN}]$.

In the 8-buck example, $f(CLK)/2^{RES(ADC)}=20M/2^{10}=19.5$ kHz (PWM frequency to match 10-bit-ADC resolution).

$LC^{1/2}/T_{UPDATE}=162\ \mu sec/25.6\ \mu sec=6.3$ (PWM adjustments within the filter time constant).

$V_{MEAS}/V_{IN}=[5\times(1\ k\Omega+1.5\ k\Omega)/1\ k\Omega]/12=1.04$ (voltage ratio measurable by ADC).

$f(PWM)<19.5\ kHz\times 6.3\times 1.04=128$ kHz (rounded up to 156 kHz in design).

Comment: Maximum PWM frequency with control resolution is equal to ADC.

APPLICATIONS AND TRENDS

Understanding and knowledge enable designers to make effective trade-offs and accelerate development. The design guidelines of the **sidebar** can help you decide whether the custom features of a digitally controlled power converter justify lower performance with a microcontroller, or added cost, power, and complexity with a DSP. The latest technology is not always the greatest, so analog may still be the better choice, depending on system requirements.

You can apply the Spice model to estimate hardware-component values and firmware parameters before building and testing. You can use it for control applications in virtually any field, including power, thermal, motion, lighting, and flow. Measure the system's open-loop step response, then adjust the model to match gain (ESWAVG) and timing (LC filter). Make RL impedance large relative to LF for a single-pole system and C_{PROC} and C_{UPDATE} negligible for an analog controller.

These tools do not address the critical of firmware development, which opens the front door to innovation and a trap door to disaster. When I published **Reference 1** in 1998 with a vision statement for the future of digital-power control, the industry expected that many tasks would be automated by now. However, designers largely face the same choice they had many years ago: Apply a limited device, or design from scratch.

Semiconductor companies continue to crank out countless variations of application-specific chips and a few "placebo" devices that let designers feel state of the art without enabling new and useful capabilities. Components are necessary to automate challenging control tasks and to enable easy customization. Until then, designers must painstakingly manage their own designs. **Reference 2** provides additional details, including useful short cuts and tips to avoid common pitfalls in digital-power control.

Power converters may be the most common electronic subsystems in the world, but they still lag other products in technological advancements. Understanding key concepts is essential in satisfying the growing demands and constraints on the power industry. With any luck, these guidelines and tools will aid in that effort. EDN

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AUTHOR'S BIOGRAPHY

David Caldwell founded Flextek Electronics in 1996 to advance digital-power control. He has an MSEE and 20 years' experience, has published more than a dozen papers, and holds two patents. He has taught professional courses in digital-power control.