

# designideas

READERS SOLVE DESIGN PROBLEMS

## Digital controller compensates analog controller

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Emerging digital ICs for power control lack basic features, such as the built-in gate drive and current limiting, that you would normally find in analog ICs. Digital-power controllers generally have only PWM (pulse-width-modulated)-logic output, and discrete gate drivers rarely include current limiting. In addition, most protected FETs work only in low-frequency, low-side applications.

The LM3485 IC from National Semiconductor ([www.national.com](http://www.national.com))

includes high-side gate drive with current limiting (Reference 1). However, the hysteretic-control scheme of this analog IC is likely to yield questionable performance in some applications due to variable switching frequency and overshoot, as well as an inability to regulate feedback below the 1.24V reference. A traditional PID (proportional-integral-differential)-control scheme can get around these limitations but adds considerable complexity.

The CLZD010 CLOZD (Caldwell-

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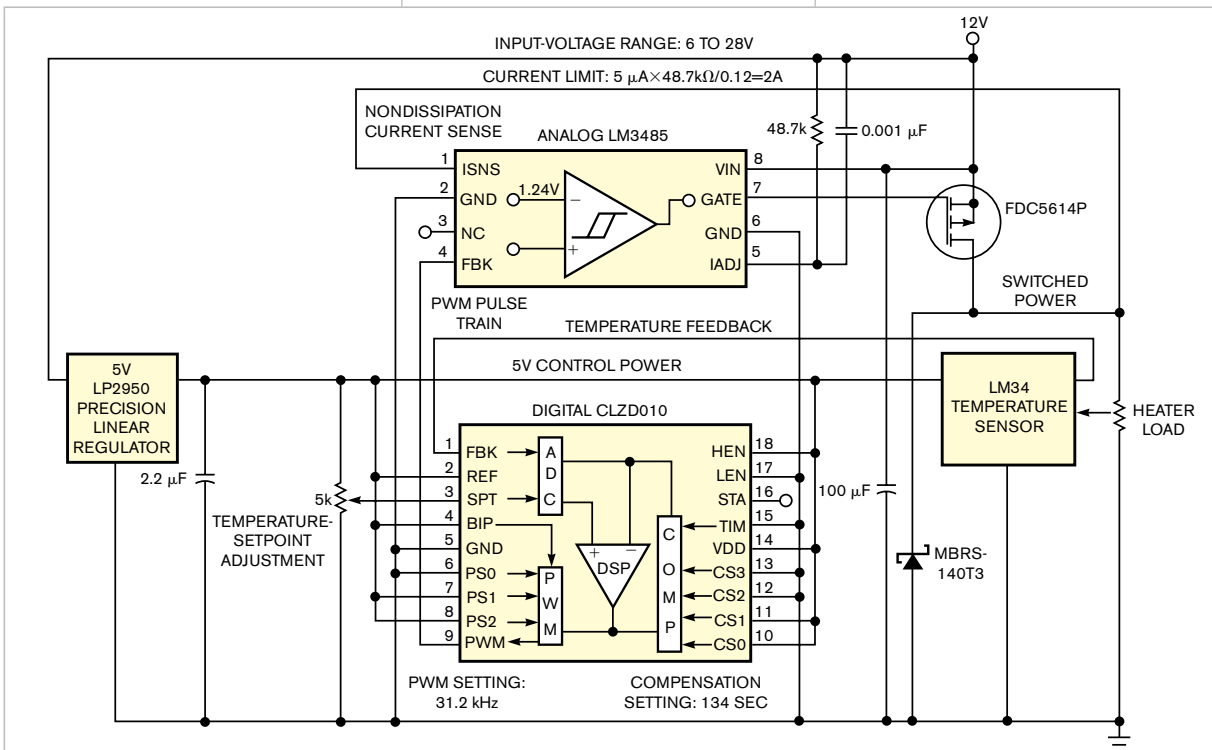


Figure 1 Combine the simple and robust closed-loop control of the digital CLZD010 with the current-limited high-side gate drive of the analog LM3485 for the best of both worlds.

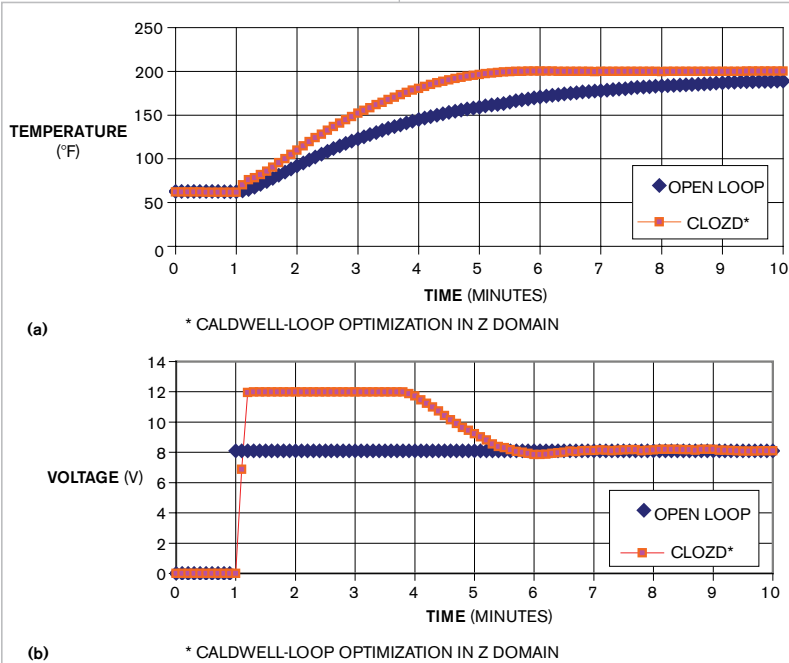
loop-optimization-in-Z-domain) controller-chip IC from Flextek Electronics ([www.flex-tek.com](http://www.flex-tek.com)) both broadens and simplifies control applications though the embedded intelligence of a digital device (Reference 2). A single time-domain compensator replaces the three frequency-domain PID pa-

rameters, eliminating complex stability analysis. The circuit requires no PC interface because you inspect the open-loop response and then use pin settings to configure the closed-loop compensation. However, the PWM output is only a logic-level driver.

Combine the simple and robust

closed-loop control of the digital CLZD010 with the current-limited high-side gate drive of the analog LM3485 for the best of both worlds (Figure 1). The PWM-logic level of the digital IC overrides the hysteretic comparator of the analog IC to switch the FET. A second comparator at ISNS, Pin 1 in the LM3485, turns off the FET if the voltage across it exceeds a predetermined value during conduction to limit current.

In the thermal-response example (Figure 2a), the circuit takes about three minutes for the open-loop temperature to reach roughly two-thirds of its final value, so closed-loop compensation, at 134 seconds, is slightly faster in Figure 1. The resultant closed-loop temperature quickly nears its final value due to maximum drive; voltage then decreases to allow the temperature to settle at the setpoint without overshoot (Figure 2b). You can use this basic circuit combination to satisfy a broad range of applications in multiple industries. **EDN**



**Figure 2** In the thermal-response example (a), the circuit takes about three minutes for the open-loop temperature to reach roughly two-thirds of its final value. The resultant closed-loop temperature quickly nears its final value due to maximum drive; voltage then decreases to allow the temperature to settle at the setpoint without overshoot (b).

## REFERENCES

- 1 "LM3485 Hysteretic PFET Buck Controller," National Semiconductor, September 2004, [www.national.com/ds/LM/LM3485.pdf](http://www.national.com/ds/LM/LM3485.pdf).
- 2 "CLOZD Loop Controller Chip, Part CLZD010," Flextek Electronics, 2004, <http://flex-tek.com/CLZD010.pdf>.

## Circuit provides constant-current load for testing batteries

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Suppose that you need to test a 1.5V, AA-size alkaline battery. You can apply a short circuit and measure current, or you can measure open-circuit voltage, but neither method properly tests the battery. A suitable test current of approximately 250 mA gives you a more reasonable test. You can use a 6Ω resistive load at 1.5V, which produces an output voltage of 1.46V at an ambient temperature of 25°C if the battery is in excellent con-

dition. A poor battery might produce less than 1.2V. Given the load, the output current at 1.2V will be 200 mA instead of 250 mA. The battery will have just 80% of a full load current. Instead, you can use the circuit in Figure 1 to produce a constant-current load.

The circuit uses a 9V battery and a voltage regulator to produce a steady power-supply voltage of 5V. From that voltage, the circuit produces a constant sink current, which is independent of

the battery's output voltage, using IC<sub>1</sub>, IC<sub>2</sub>, and Q<sub>3</sub>. Your choice of current depends on battery size. You calculate the sink current of this circuit as  $I_{TEST} = 1/R_{19} \times [V_{CC} \times R_{18} / (R_4 + R_{18})]$ , where  $I_{TEST}$  is the current you are testing and  $V_{CC}$  is the voltage of resistive divider R<sub>4</sub> and R<sub>18</sub>. The voltage across R<sub>19</sub> should range from 0.3 to 0.85V for AAA and AA batteries. Transistor Q<sub>3</sub> should be in its active region. Resistor R<sub>14</sub> limits Q<sub>3</sub>'s base current to a safe level.

A suitable choice for the operational amplifier, IC<sub>2</sub>, is also important. You should use a single-supply op amp with a rail-to-rail input and a rail-to-rail output, such as Analog Devices' ([www](http://www).

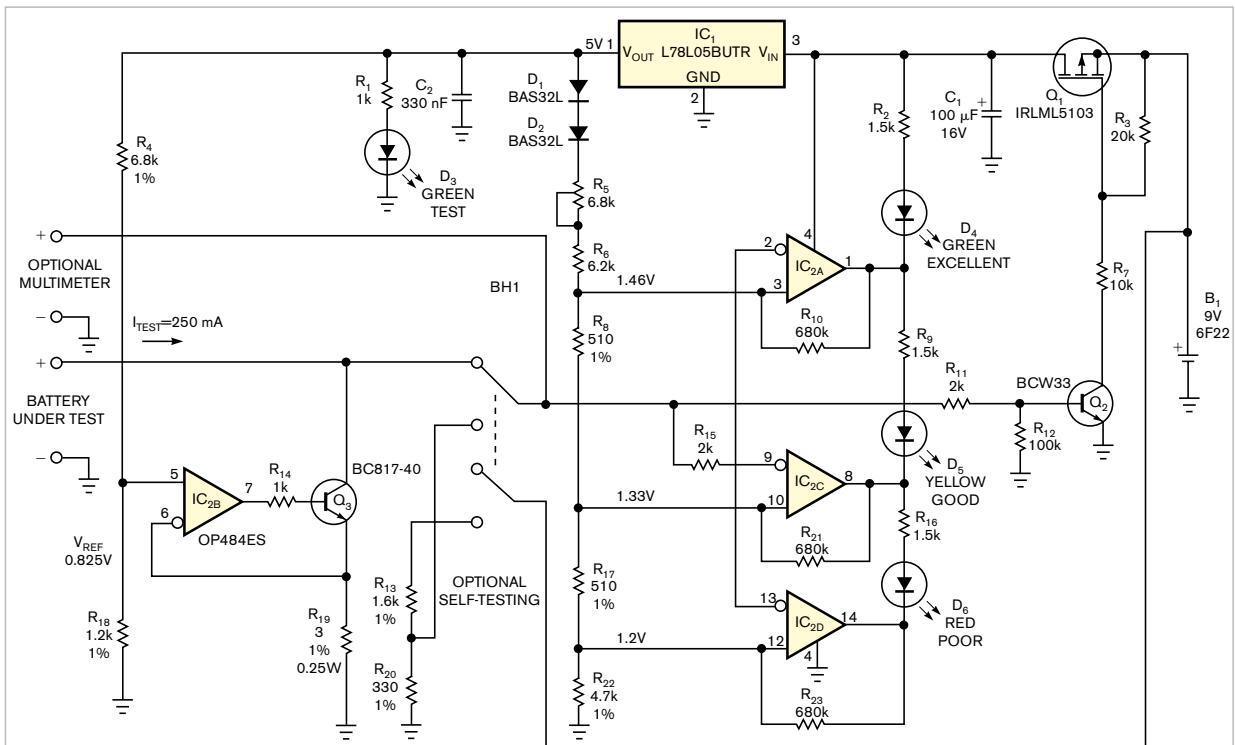


Figure 1 A tester of AA- or AAA-sized batteries uses constant-current load.

TABLE 1 VOLTAGE RANGES FOR LEDs

Condition	Battery voltage <sup>1</sup> (V)	D <sub>2</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>3</sub>
Excellent	>1.46	Yes	Yes	No	No	Yes
Good	>1.33	Yes	No	Yes	No	Yes
Poor	>1.2	Yes	No	No	Yes	Yes
Bad	>1 <sup>2</sup>	Yes	No	No	No	Yes
Unable to test	>12	No	No	No	No	No

<sup>1</sup>Ambient temperature is 25°C.

<sup>2</sup>This estimated value can be less.

analog.com) OP484ES or OP496GS.

When you connect the battery under test, Q<sub>2</sub> turns on, which then turns on Q<sub>1</sub>, applying voltage from the 9V battery to the regulator. That action lights D<sub>3</sub>, indicating that the battery under

test has enough voltage to be tested. LEDs D<sub>4</sub>, D<sub>5</sub>, and D<sub>6</sub> indicate the battery's condition. Table 1 shows the voltage ranges necessary for these LEDs to light.

Op amps IC<sub>2A</sub>, IC<sub>2C</sub>, and IC<sub>2D</sub> work as comparators with some hysteresis for operational stability. The resistive divider comprising R<sub>5</sub>, R<sub>6</sub>, R<sub>8</sub>, R<sub>17</sub>, and R<sub>22</sub> sets the voltage levels. Diodes D<sub>1</sub> and D<sub>2</sub> are optional but are useful when you need to operate the circuit outdoors, where temperatures vary widely. Resistor R<sub>15</sub> protects the inputs of IC<sub>2A</sub>, IC<sub>2C</sub>, and IC<sub>2D</sub>.

When you connect a battery to test, you should test it for at least 5 seconds. LED D<sub>3</sub> shines if the battery is in relatively normal condition. In this case, switch Q<sub>1</sub> applies power to the battery tester. The sink-current generator comprising IC<sub>2A</sub> and Q<sub>3</sub> loads the battery under test, and the resistor-divider network sets the comparator voltages.

You can add an optional self-testing button for checking the 9V battery to ensure that it has enough voltage to drive the circuit. You can also connect a digital multimeter to the multimeter terminals if you need a more accurate measurement. You can use a suitable rotary switch or a variable resistor and change the value of the test current by changing the value of R<sub>4</sub> to test another type or size of battery. EDN

## MOSFET-based, analog circuit calculates square root

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Square-root-calculating circuits find wide use in instrumenta-

tion and measurement systems for such tasks as calculating the rms (root-

mean-square) value of an arbitrary waveform, for example. Hence, designers need an effective analog square-root calculator. Because manufacturers do much of the IC fabrication in MOS technology, a MOSFET-based, analog square-root calculator seems appropri-

ate. This Design Idea describes such a circuit, which uses only MOSFETs to provide the square-root function (**Figure 1**). The design is simple and versatile and can provide the output as the square root of the difference of two voltages.

The circuit uses the nested connection of MOSFETs  $Q_1$  and  $Q_2$ .  $Q_2$  works in the saturation region as it is diode-connected, forcing  $Q_1$  to work in the triode region. All other MOSFETs work in the triode region. The first part of the circuit, comprising  $Q_3$ ,  $Q_4$ ,  $Q_5$ , and  $Q_6$ , creating the current  $I_{O1}$ , is basically a MOS-resistive circuit. The essential **equation** governing the circuit operation is:

$$V_O = \left( \sqrt{\frac{1}{K_2}} - \sqrt{\frac{1}{K_1}} \right) \sqrt{I_{O1}}$$

where  $K_1$  and  $K_2$  represent the aspect ratios of transistors  $Q_1$  and  $Q_2$ , respectively:  $K_1 = (\mu C_{OX} W)/2L_1$ , where  $I = K_1 = K_2$ . The MOSFETs creating the MOS-resistive circuit and hence responsible for the current creation are identical, having the same aspect ratio and threshold voltage. The current relates to inputs  $V_1$  and  $V_2$ , as the following **equation** shows:  $I_{O1} = G(V_1 - V_2)$ , where  $G = 2K(V_A - V_B)$  and represents the conductance of the MOS-resistive circuit— $k = (\mu C_{OX} W)/2L$ —of

the identical transistors forming the MOS-resistive circuit, and  $V_A$  and  $V_B$  are control voltages applied to the gate of the MOSFETs that are working in the triode. This approach provides the advantage of voltage controllability of the output; hence, the square-rooting function is voltage-controllable.

The following **equation** gives the output voltage:

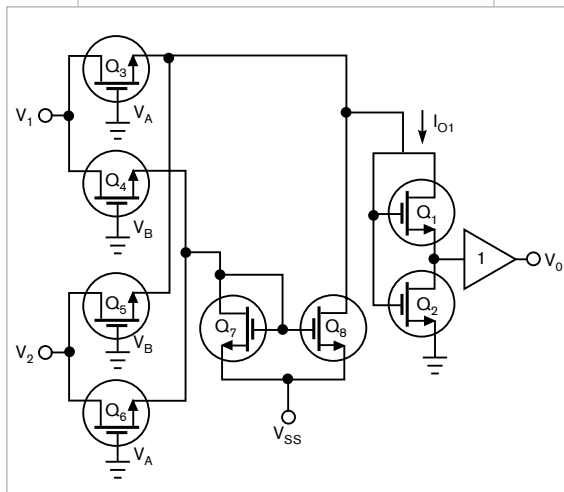
$$V_O = 2 \left( \sqrt{\frac{1}{K_1} + \frac{1}{K_2}} - \sqrt{\frac{1}{K_2}} \right) \times \sqrt{K(V_A - V_B)(V_1 - V_2)}$$

It is evident from this equation that the output voltage,  $V_O$ , is the square

root of the difference of input voltages  $V_1$  and  $V_2$ . If you ground  $V_2$ , then the output voltage is proportional to the square root of input voltage  $V_1$ . As noted, control voltages  $V_A$  and  $V_B$  can vary the proportionality constant. Hence, you have devised a new all-MOSFET-based, voltage-controllable analog square-root calculator.

You can test the circuit using a variety of commercially available MOSFETs, such as the 2SK1228, which is available from many sources; the buffer can be a MOSFET-based op-amp buffer, such as the BUF04701 from Texas Instruments ([www.ti.com](http://www.ti.com)). For the operation of the circuit to be in accordance with the output-voltage **equation**, the four MOSFETs you use


to create the MOS-resistive circuit should be identical and should work in the triode region, for which inputs  $V_1$  and  $V_2$  should be less than  $V_A - V_{TH}$  and  $V_B - V_{TH}$ , respectively. The MOSFETs in the current mirror,  $Q_7$  and  $Q_8$ , should be identical, and the diode-connected MOSFETs,  $Q_1$  and  $Q_2$ , should be different and have different aspect ratios. You can test the circuit onboard using commercially available ICs, or you can simulate it on a computer using any standard version of Spice. The supply voltage must be in accordance with the selected components. **EDN**



**Figure 1** This circuit uses only MOSFETs to provide the square-rooting function.

## “Hippasian” nonlinear VFC stretches dynamic range

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 Hippasus of Metapontum was a Greek philosopher who lived approximately 500 BC. A disciple of Pythagoras, Hippasus discovered some interesting properties of square roots. This Design Idea describes a VFC (voltage-to-frequency converter) that also uses an interesting property of square roots: their ability to

extend VFC dynamic range by orders of magnitude (**Figure 1**).

Linear VFCs are one of the oldest types of ADCs, and their simplicity and noise rejection preserve their popularity. However, their Achilles’ heel is the direct proportionality between dynamic range and conversion time. Because the voltage resolution

of linear VFC conversion is equal to the full-scale voltage reference,  $V_{REF}$  divided by full-scale frequency,  $f_{FS}$ , multiplied by the counting interval, large dynamic range is inevitably associated with long counting intervals and slow conversion, even when clever VFC design provides for fast full-scale frequency.

For example: If you use a 3-MHz VFC-based ADC, such as Analog Devices’ ([www.analog.com](http://www.analog.com)) AD7742 with a 2.5V reference voltage in a design that requires 1-mV resolution, then

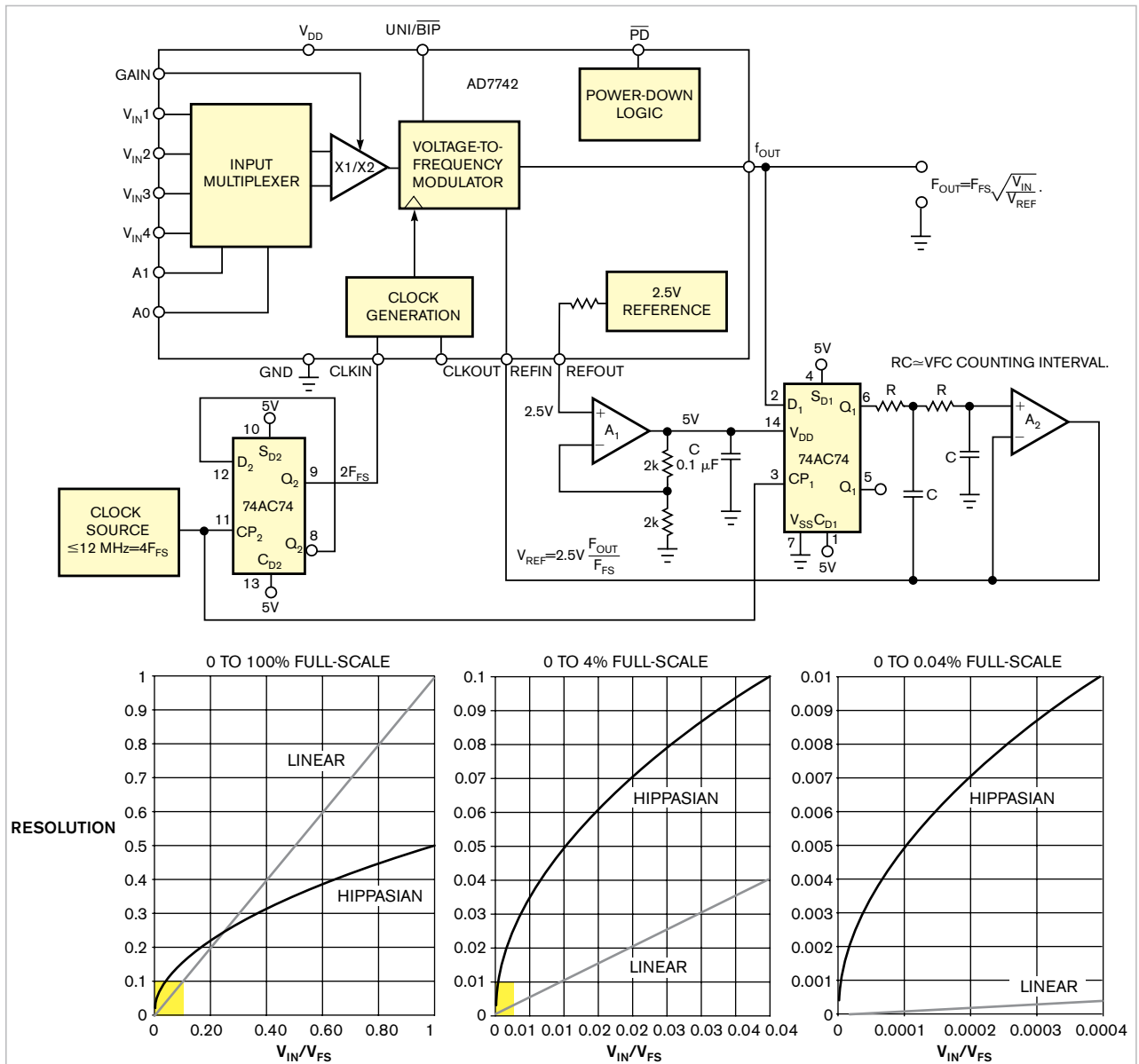


Figure 1 This nonlinear, wide-dynamic-range voltage-to-frequency converter exhibits 25-times improvement in counting time over other approaches.

you would need a minimum counting interval of  $2.5/1 \text{ mV}/3 \text{ MHz} = 2500/3 \text{ MHz} = 833 \mu\text{sec}$ . That counting interval yields only 1200 conversions per second, which for many applications is inconveniently slow.

The “Hippasian” VFC avoids this problem with a semiparabolic-transfer function instead of a linear one. It works by substituting  $V_{REF2}$ , which, instead of the constant  $V_{REF}$  of a linear VFC, is proportional to the output frequency. Then,  $V_{REF2} = V_{REF} \times f_{OUT}/f_{FS}$ ,

$$f_{OUT} = V_{IN} \times f_{FS} / V_{REF2} = V_{IN} \times f_{FS} / (V_{REF} \times f_{OUT} / f_{FS}), (f_{OUT} / f_{FS})^2 = V_{IN} / V_{REF} \text{ and } f_{OUT} = f_{FS} \times (V_{IN} / V_{REF})^{1/2}.$$


Generating the dynamic, output-frequency-proportional reference voltage is the job of op amps  $A_1$ , which boosts the VFC’s internal 2.5V reference to power flip-flop  $Q_1$ , and  $Q_1$  and  $A_2$ , which compose a high-performance frequency-to-voltage converter. The accuracy of the reference voltage depends on precise 50-to-50 symmetry of the VFC’s input-clock reference. Flip-

flop  $Q_2$  guarantees this symmetry.

The effect on conversion resolution of low-level signals is dramatic. To return to the example of a 2.5V full-scale, 1-mV-conversion resolution, which requires a 2500-count, 833- $\mu\text{sec}$  conversion interval with a linear 3-MHz VFC, the Hippasian version needs only 100 counts and 33  $\mu\text{sec}$ —a 25-fold improvement. Software linearization of the Hippasian VFC conversion is easy, requiring only one multiplication. **EDN**

# Decoder lights the way

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 To display the status of two digital outputs, you can simply connect an LED and its resistor on each output. You must, however, interpret, or “decode,” the displayed binary code. In addition, when no LED lights, users have no way of knowing whether it means that both outputs are off, that the power is off, or that a malfunction has occurred. In some applications, including industrial and medical settings, an indicator sending an ambiguous signal would be unacceptable. This Design Idea describes a simple circuit

that resolves this problem by displaying four states on four LEDs (**Figure 1**). The operator need not understand binary coding, and, if no or more than one LED lights, it can mean only “no power” or “default.”

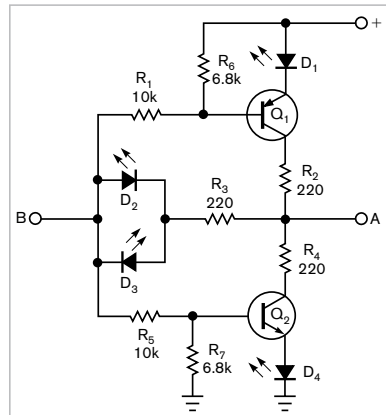
The circuit works in the following way: If both inputs A and B are low,  $Q_1$  allows current to pass through  $D_1$  and resistor  $R_2$  to A; only  $D_1$  will light. Symmetrically, if both inputs A and B are high,  $Q_2$  passes, and the current can pass from A through  $R_4$ ,  $Q_2$ , and  $D_4$ ; only  $D_4$  will light. If both inputs

**TABLE 1 LED-LIGHTING POSSIBILITIES**

IN		LED			
A	B	1	2	3	4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

are on different levels, only  $D_2$  or  $D_3$  will light. **Table 1** shows the possibilities; all other displays point to a default, such as a bad connection, a no-power condition, or a malfunction.

A totem-pole output that can sink and source



**Figure 1** This simple circuit displays four states on four LEDs.

the current for one LED must drive the A and B inputs. Resistors  $R_2$ ,  $R_3$ , and  $R_4$  are for applying a 12-mA LED current if the power supply is 5V. No component is critical. For example, you can use generic transistors, such as the NPN 2N3904 and the PNP 2N3906. You can even use transistors with integrated base resistors, further reducing the component count. **EDN**