

2.0 CLOZD™ Loop Controller Chip

Part CLZD010

CLOZD™ (Caldwell Loop Optimization in Z-Domain) is a low-cost digital closed-loop control chip developed by Flextek Electronics for simplicity, robustness, and versatility. Just select the desired control configuration through pin settings and quickly close a loop around a power supply, motor drive, lamp, heater, fan, valve, actuator, transmitter, transformer, regulator or virtually anything that needs to be controlled. Minimal experience is required since this is the simplest closed-loop controller in the world.

Highlights:

- Control Systems from 128uS to 1,074S
- Effective 12Bit Control Resolution
- PWM Drive from 488Hz to 62.5KHz
- Bipolar Option for Full-Bridge Drive
- Triac Option for Off-Line Applications
- Open Loop Option for Characterization
- Built-In Operational Limits
- Digital Filtering and Protection
- Replaces Countless Parts
- No Programming Required
- Extremely Easy-to-Use and Extremely Flexible
- Many Advantages over Traditional PID Control

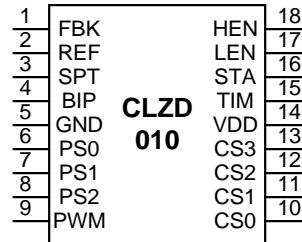


Figure 2.1. CLZD010
18 Pin DIP Package

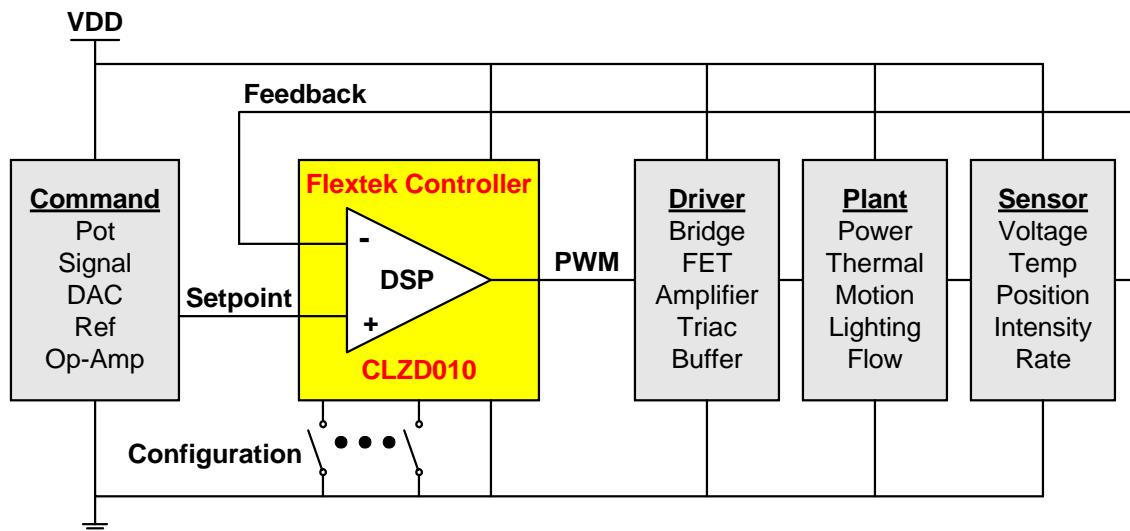


Figure 2.2. CLOZD™ Loop Controller System Application Diagram

Overview

CLOZD™ Loop Controller utilizes advanced Digital Signal Processing (DSP) techniques and algorithms to satisfy challenging real-time control applications quickly and easily. The PWM drive of the controller is automatically adjusted until the measured Feedback sensor signal matches the desired Setpoint command. Configure the controller for a broad range of power, thermal, motion, lighting, and flow applications by selecting appropriate pin settings.

Patent 6697685

This flexible closed-loop controller benefits customers by using the same component in a variety of applications. Parts not only cost less when purchased in volume, but development time is reduced by re-applying familiar technology, and using proven components increases reliability.

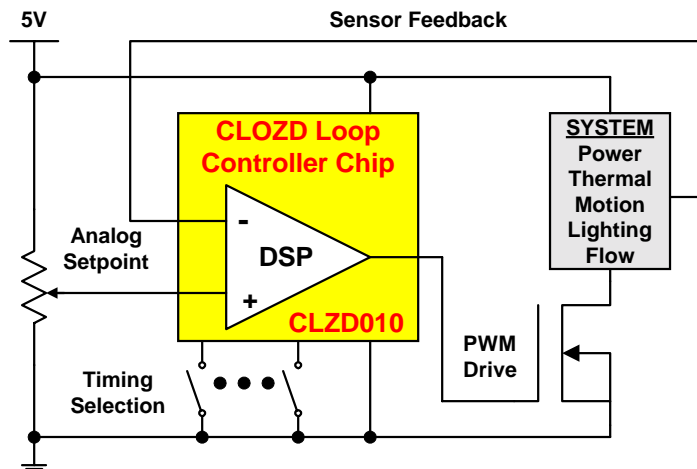
Operation

Closed-loop controllers make automatic adjustments to maintain constant output despite varying conditions. Examples include supply voltage, fluid temperature, motor speed, and light intensity. These parameters would shift over time and load without consistent correction.

Microcontrollers executing firmware are replacing op-amps with feedback networks that used to perform closed-loop control. These digital implementations are versatile but time-consuming to program, and control demands often exceed processor resources. Considerable expertise is required to properly design a system to avoid oscillations or sluggish response. Additionally, we naturally observe events in the time-domain while control analysis is typically done in the frequency-domain, which can be complex and confusing.

One solution to these challenges is an automated closed-loop controller configured by intuitive time-domain settings. CLOZD™ is a patented control chip developed by Flextek Electronics that is versatile and easy to use. Just select the desired timing configuration through pin settings and quickly close a loop around a power supply, motor drive, lamp, heater, fan, Peltier, valve, actuator, or amplifier.

Controller drive is automatically adjusted until the measured sensor signal matches the desired command. The Digital-Signal-Processing (DSP) algorithms within the CLZD010 control chip compare the feedback sensor signal and the analog setpoint command to determine appropriate Pulse-Width-Modulator (PWM) drive for the plant. Typical plants include power, thermal, motion, lighting, and flow applications.



Closed loop control may be the most common and yet the most challenging task in electronics. By automating this task with versatile interfaces that are easy to use, a wide range of custom applications are quickly satisfied. Users save time and money by quickly configuring the same components for multiple applications. This allows savings on parts by purchasing in volume, reduced development time by reapplying familiar technology, and increased reliability by using proven components.

CLOZD™ Loop Controller utilizes advanced Digital Signal Processing (DSP) techniques and algorithms to satisfy challenging real-time control applications quickly and easily. Other methods and products require extensive programming and complex frequency-domain analysis.

Specifications

Parameter	Specification
VDD Voltage	4.5V to 5.5V
VDD Current	1.5mA Typical
VDD Brownout Reset	<4V for 100uS
Operating Temperature	-25C to 85C
ADC Reference Voltage	2.4V to VDD
ADC Reference Current	160uA Typical
ADC Resolution	10 Bit Hardware / 12 Bit Software Enhanced
Digital Output Drive	25mA Maximum
Digital Input Levels	LO < 0.8V & HI > 2.4V

Figure 2.3. CLOZD™ Loop Controller Specifications

Description

Pin	Name	Type	Description	Comment
1	FBK	Analog Input	Feedback Sensor Signal	GND to REF Range
2	REF	Analog Input	Reference for Analog Section	2.4V to VDD Range
3	SPT	Analog Input	Setpoint for Desired Operation	GND to REF Range
4	BIP	Digital Input	Bipolar PWM Option	HI = 50% Init PWM
5	GND	Power Return	Ground	Ground
6	PS0	Digital Input	PWM Frequency Select Bit 0	LSB
7	PS1	Digital Input	PWM Frequency Select Bit 1	
8	PS2	Digital Input	PWM Frequency Select Bit 2	MSB
9	PWM	Pulsed Output	Pulse Width Modulator Output	Servo Drive
10	CS0	Digital Input	CLOZD Timing Select Bit 0	LSB
11	CS1	Digital Input	CLOZD Timing Select Bit 1	
12	CS2	Digital Input	CLOZD Timing Select Bit 2	
13	CS3	Digital Input	CLOZD Timing Select Bit 3	MSB
14	VDD	Power Supply	5V Power	4.5V to 5.5V Range
15	TIM	Digital Input	Timing Range	HI = High Rate
16	STA	Digital Output	Status Output	Hi = Enabled
17	LEN	Analog Input	Low Enable	Threshold = REF/4
18	HEN	Analog Input	High Enable	Threshold = REF/4

Figure 2.4. CLOZD™ Loop Controller Pinout

REF: ADC reference for analog section (SPT, FBK, LEN, and HEN) allows greater sensitivity for low-level signals or insensitivity to VDD variations. Can be tied to VDD for most applications.

FBK: Feedback analog sensor signal from plant under control. FBK is not used in “Open Loop” mode (CS3-CS0=1). Low source impedance <2K Ω is recommended for maximum accuracy (12 Bit) but <10K Ω is sufficient for most applications (10 Bit).

SPT: Setpoint analog command for desired level of plant feedback sensor signal. Low source impedance <2K Ω is recommended for maximum accuracy (12 Bit) but <10K Ω is sufficient for most applications (10 Bit).

LEN & HEN: Low enable must be below threshold (REF/4) and high enable must above threshold to run chip. Can serve as analog limits for current, temperature, or power supply voltage. STA and PWM outputs are low while chip is disabled. PWM duty cycle is reset to zero (or 50% if BIP=1) when the chip is re-enabled. Enable inputs are sampled every 512uS.

STA: Digital output status is high when chip is active ($VDD > 4.5V$, $LEN < REF/4$, and $HEN > REF/4$) or low when chip is disabled.

Set	PS2	PS1	PS0	Mode	Frequency	Resolution
7	1	1	1	PWM	62.5 KHz	7 Bit
6	1	1	0	PWM	31.2 KHz	8 Bit
5	1	0	1	PWM	15.6 KHz	9 Bit
4	1	0	0	PWM	7.81 KHz	10 Bit
3	0	1	1	PWM	1.95 KHz	10 Bit
2	0	1	0	PWM	488 Hz	10 Bit
1	0	0	1	TRIAC	120 Hz	7 Bit
0	0	0	0	TRIAC	100 Hz	7 Bit

Figure 2.5. PWM Drive Frequency and Mode Settings

PWM: Output drive signal is pulse width modulated to adjust power delivered to the plant (Figure 2.19). This signal is adjusted from zero to 100% duty cycle, except in triac mode when the phase of a fixed duration pulse is adjusted (Figure 2.15). PWM is low when chip is disabled.

PS2-PS0: PWM frequency select pins to configure output drive for various plants (Figure 2.5). Lower frequencies reduce switching loss in slower applications (Figure 2.8), while higher frequencies reduce inductor size and eliminate audio buzz in power applications (Figure 2.12), and triac mode enables high power control at minimal cost in off-line applications (Figure 2.14).

BIP: Bipolar mode initializes the PWM duty cycle to 50% when BIP is pulled high to VDD, allowing anti-phase full-bridge drives to start at zero power (Figure 2.17). Normally this pin is pulled low to GND for zero initial duty cycle, but it can be used to speed loop acquisition when high drive levels are expected (Figure 2.9).

TIM: Timing range select for closed-loop control. Pull up to VDD (TIM=1) for higher rate in faster systems such as power, or pull down to GND (TIM=0) for lower rate in slower systems like thermal. High rate is only available for PWM frequencies of 7.81KHz and above (PS2=1). TIM is used for phase detection in triac circuits (Figure 2.14) where only low rate control is available.

CS3-CS0: Control timing select pins to configure loop for plant time constant (Figure 2.6). Estimate timing of plant from data sheet or open loop response. Too fast of a setting will overshoot or oscillate and too slow of a setting will be overly sluggish or oscillate. All pins tied to VDD selects "Open Loop" mode where the PWM drive is proportional to the SPT command.

Set	CS3	CS2	CS1	CS0	CLOZD (TIM=1)	CLOZD (TIM=0)
15	1	1	1	1	Open Loop	Open Loop
14	1	1	1	0	128 uS	65.5 mS
13	1	1	0	1	256 uS	131 ms
12	1	1	0	0	512 uS	262 mS
11	1	0	1	1	1.02 mS	524 mS
10	1	0	1	0	2.05 mS	1.05 S
9	1	0	0	1	4.10 mS	2.10 S
8	1	0	0	0	8.19 mS	4.19 S
7	0	1	1	1	16.4 mS	8.39 S
6	0	1	1	0	32.8 mS	16.8 S
5	0	1	0	1	65.5 mS	33.6 S
4	0	1	0	0	131 mS	67.1 S
3	0	0	1	1	262 mS	134 S
2	0	0	1	0	524 mS	268 S
1	0	0	0	1	1.05 S	537 S
0	0	0	0	0	2.10 S	1,074 S

Figure 2.6. Control Timing Settings

Advantages

CLOZD™ may be configured quickly and easily for effective results, compared to traditional algorithms that require complex analysis or unreliable tuning to produce questionable results with excessive components.

CLOZD™	PID
Developed specifically for digital control	Derived from traditional analog approach
Optimized for micro firmware execution	Approximation of op-amp circuit
Intuitive time domain characterization	Complex frequency domain characterization
Single adjustment parameter	Three interacting adjustment parameters
Highly controllable	Integral wind-up and Differential sample problems
Robust operation	Oscillation susceptible and noise sensitive
Amenable to auto-tune or adaptive	Challenging to automate

Figure 2.7. CLOZD™ vs. PID for Closed-Loop Control

Limitations

The versatility of CLOZD™ is demonstrated through numerous application examples. However, no single device can satisfy every requirement of every application, so users must thoroughly test their system in a safe manner before committing to production. Customers are ultimately responsible for their own designs and Flextek makes no warranties, expressed or implied.

Applications

Thermal control systems are challenging because they have low-level signals, long time constants, and multiple lag elements that can cause overshoot. However, this one is quick and easy to configure for high performance with a few inexpensive parts.

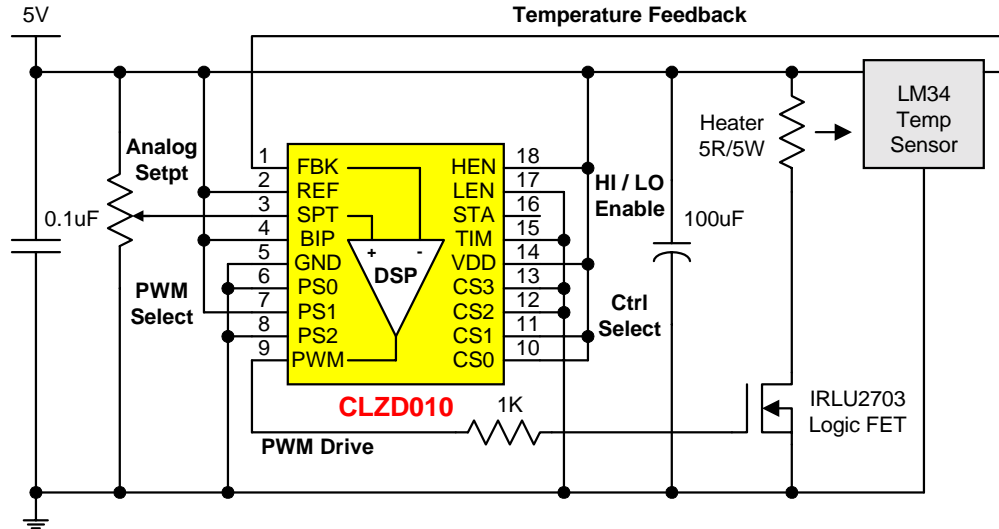


Figure 2.8. Thermal Controller (5W Heater)
 PWM = 488Hz (PS=010, BIP=1)
 CLOZD = 134S (CS=0011, TIM=0)

The logic FET can be driven directly because low frequency PWM (PS2-PS0=488Hz) is used with slow transitions (1KΩ gate resistor). The bipolar option was not required but quickened loop acquisition by starting with a higher drive level (PWM=50% at start-up if BIP=1).

Control timing was estimated by applying power to the heater and monitoring the temperature response. It took over ten minutes for temperature to settle near its final value in this open loop configuration. The temperature went from ambient to about two thirds of its final value in two to three minutes ($\tau = 1 - e^{-1} \approx 63\%$), so the timing of the system was set slightly faster (CS3-CS0=134S).

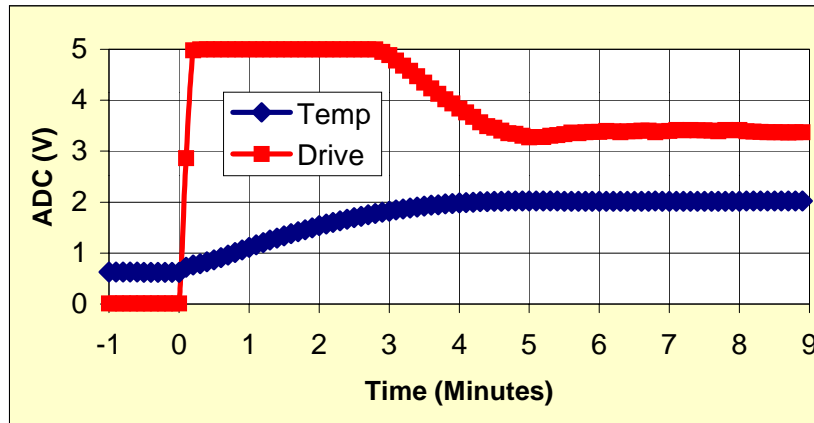


Figure 2.9. Temperature Feedback and Filtered PWM Drive Captured by FlexController™

Most scopes are too slow to capture a thermal response so FlexController™ was used as a logger with the data exported to Excel. The drive is high while the loop error (FBK-SPT) is large but decreases prior to the temperature reaching its final value of 200°F (FBK=2V) for fast response without overshoot.

This switching power amplifier can source or sink current and may serve as a versatile microcontroller commanded DC/DC converter. The interface shown is a DAC with SPI serial port, but I²C could be used as well. All the command circuits in these application examples are interchangeable.

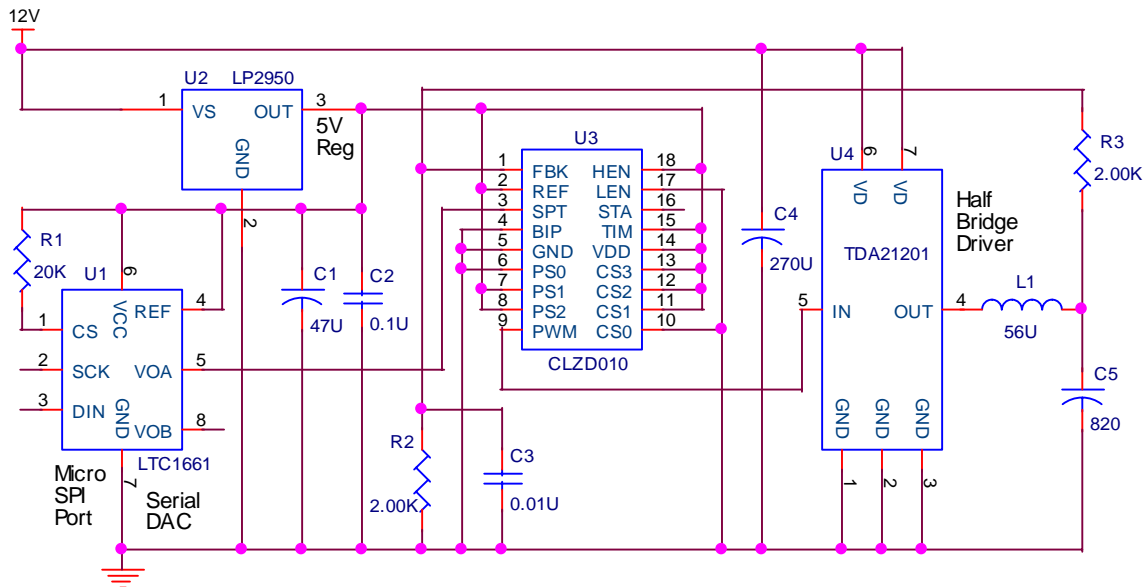


Figure 2.12. Switching Power Amplifier (10V/5A Voltage Converter) with Micro Interface
 PWM = 31.2KHz (PS=110, BIP=0)
 CLOZD = 128uS (CS=1110, TIM=1)

The LC filter response is fast and susceptible to ringing so high speed sampling and control calculations are required. For this reason, the 128uS control setting is used despite the 214uS time constant of the system ($\tau = LC^{1/2}$).

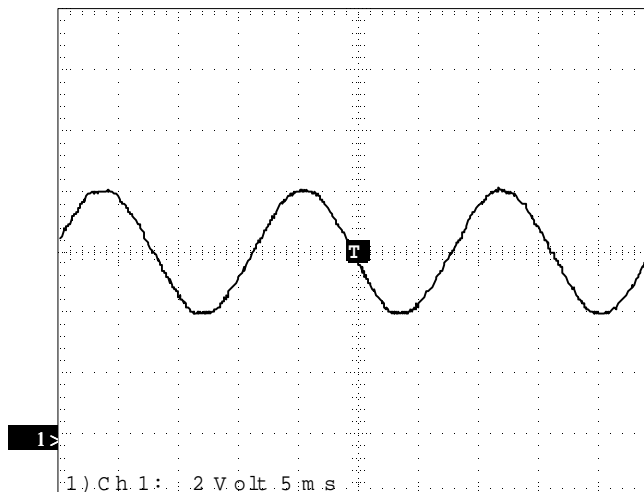


Figure 2.13. Output Voltage of Converter with 60Hz Sine Setpoint

This triac circuit maintains constant light intensity despite variations at the sensor location. It is small and inexpensive because load and housekeeping power are derived directly from line voltage, eliminating bulky expensive supplies. The circuit can be changed to control a heater, and is available at 50Hz (PS2-PS0=100Hz Triac since operation repeats every half cycle).

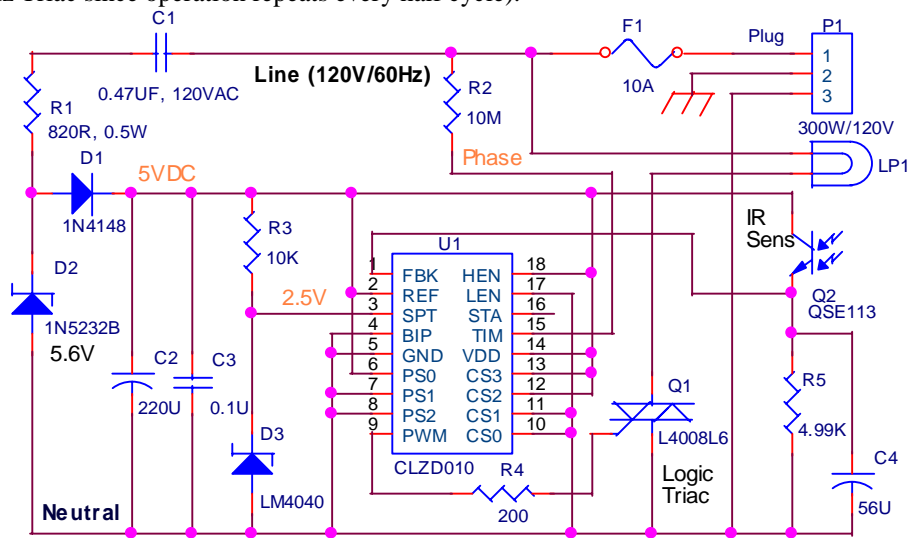


Figure 2.14. Off-line Light Controller (120V Incandesant)

PWM = 120Hz Triac (PS=001, BIP=0)

CLOZD = 262ms (CS=1100, TIM=Phase)

Caution: High Voltage Application for Experienced Professionals Only

The timing of this circuit is a function of the RC filter ($\tau = 4.99K\Omega \cdot 56\mu F = 279ms$) used to smooth the 120Hz light sensor output. Limited filtering is required since CLOZD™ utilizes oversampling and digital filtering to enhance control resolution. The 5V supply can be used as the analog reference even if it varies because it does affect the setpoint (fixed reference) or feedback (current source). The drive is adjusted until FBK and SPT are equal, so control accuracy is based on relative measurements rather than absolute values.

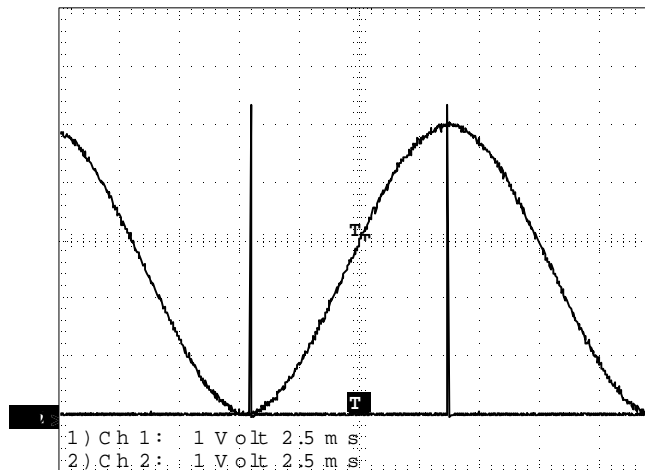


Figure 2.15. Scaled Line Voltage with Triac Gate Pulse at Half Power

The triac gate is pulsed for approximately 100uS to turn on the load for the remainder of the half-cycle, so higher power is achieved by turning on earlier in the half-cycle. The phase timing (zero-crossing of line voltage) is derived from a logic level at the TIM pin (only low rate timing available in triac mode).

This thermal control circuit is unique in that it is bipolar (heating or cooling). A Peltier cell (or TEC) driven by a full-bridge enables this versatility. This circuit uses high frequency switching to reduce magnetics and buzz, and utilizes the same timing as the heater circuit in Figure 2.8.

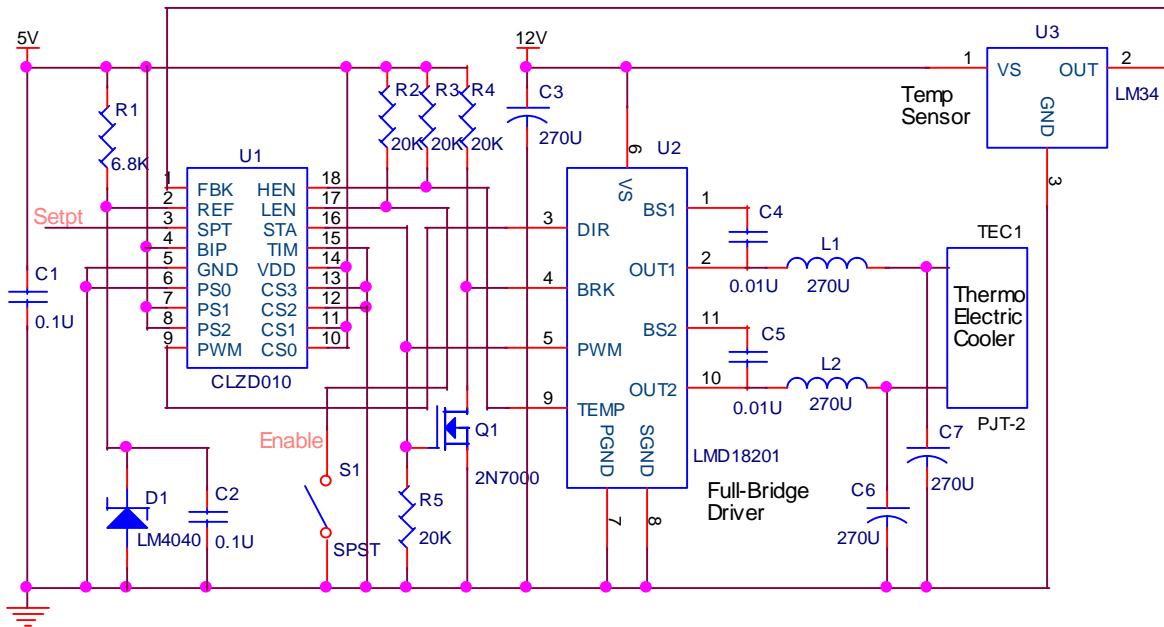


Figure 2.16. Bipolar Thermo-Electric Cooler (12V/3A Peltier Cell)
 PWM = 31.2KHz (PS=110, BIP=1)
 CLOZD = 134S (CS=0011, TIM=0)

A precision voltage reference is used to sense low temperatures with high sensitivity. If the control chip is disabled, its status pin will shut down the power stage (requirement since PWM is low during disable). Likewise, the over-temp warning of the power stage will to shut down the control chip if necessary.

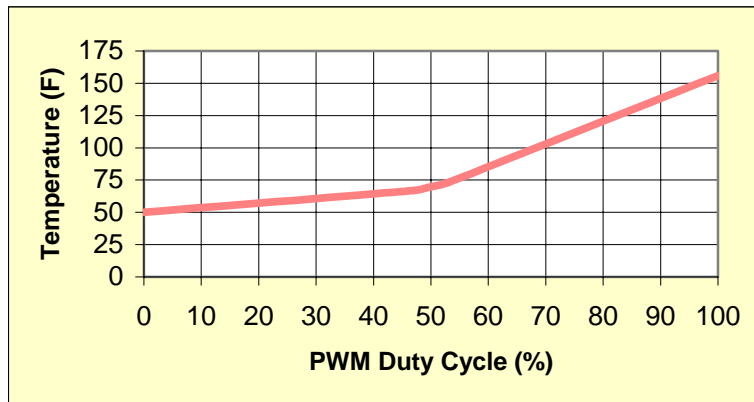


Figure 2.17. TEC Thermal Response to Full-Bridge Duty Cycle

The BIP pin is tied high to start at 50% duty cycle which delivers no power to the load since both sides of TEC are at half of the supply voltage. Figure 2.17 illustrates that room temperature is measured at 50% duty cycle, with heating above that and cooling below. This TEC orientation is required for negative feedback since the controller expects the feedback signal to rise with drive (higher duty cycles result in higher temperatures). Notice the shallow slope of the curve below 50% due to the less efficient cooling of the TEC relative to heating. This slope difference affects the gain of the control loop but is not a problem for the CLOZD™ algorithm.

This circuit maintains constant motor velocity despite variations in load and supply.

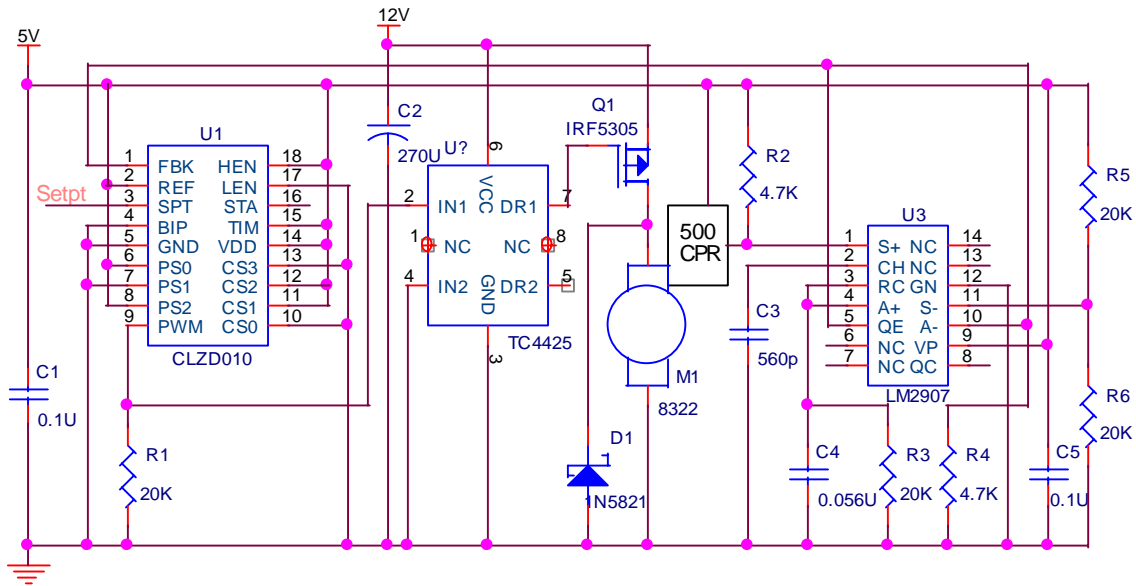


Figure 2.18. DC Brush Motor Speed Control
 PWM = 15.6KHz (PS=110, BIP=0)
 CLOZD = 32.8mS (CS=0011, TIM=1)

The data sheet for this motor stated a 15mS mechanical time constant, but more robust operation was observed over varying operating conditions with 32.8mS timing. The 1mS filtering of the frequency-to-voltage converter chip is much faster than the motor so it only contributes a small lag.

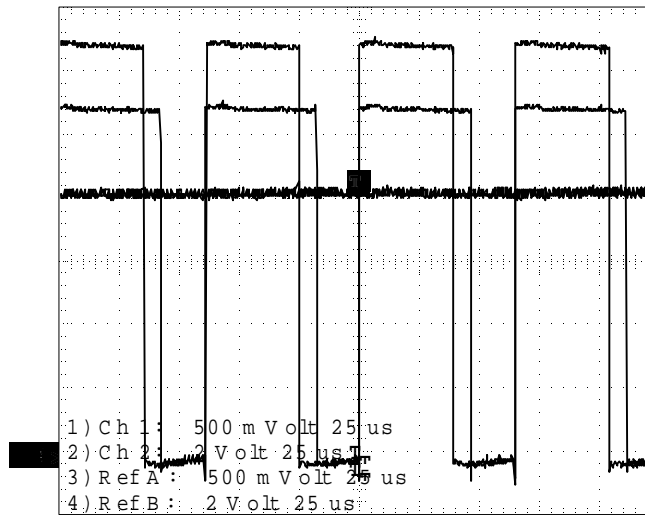


Figure 2.19. PWM Drive and Velocity Feedback with 11V and 13V Supply Voltages

Figure 2.19 illustrates that more drive (higher duty cycle) is required at a lower supply voltage to maintain constant power to the motor, which is required for constant speed with the same load. Loading the motor, without varying supply voltage, will also cause the drive to increase duty cycle.