

8-BUCK Converter Design Kit
Learn Digital Power through Hands-On Example
Flextek Electronics
www.flex-tek.com

Overview

Kit enables customer to build, program, test, and analyze a Buck converter controlled by an 8-bit PIC Micro. Efficient design practices illustrate key concepts in simple terms that apply to a broad range of technologies. Kit includes blank PCB, programmed chip, and documentation with schematic, parts list, description, SPICE model, and assembly source code. Converter featured in EDN "Power Goes Digital" 8/18/5 tutorial and Professional Advancement Courses at Power Systems World 2005.

Contents

- Blank PCB with parts list for customer assembly (text file included for quick upload at DigiKey)
- PIC Micro programmed with power conversion code (firmware equipment and experience not required)
- Assembly source code with license to distribute machine code in programmed chips
- Documentation for hardware, firmware, and basic operation including supporting articles:
 - "Power Goes Digital," EDN Magazine, Aug. 18, 2005
 - "Microcontroller Enables Digital Control in SMPS," Power Electronics Magazine, Feb. 2004
 - "Power Control: Digital Flexibility at Analog Prices," PSW Paper, Nov. 12, 1998

Benefits

- Flextek original technology to advance emerging field of digital power control
- Valuable principles are universal to other devices and applications
- Demonstrate capabilities and limitations of digital power essential to effective trades
- Flextek grants customer license to program PIC Micro chips with compiled machine code

Limits

- Customer agrees not to disclose firmware source code (each user purchases own kit)
- Proven firmware is commented and illustrated but not covered by product support
- Flextek consultation not included in kit purchase (available at additional cost)
- Flextek makes no warranties expressed or implied

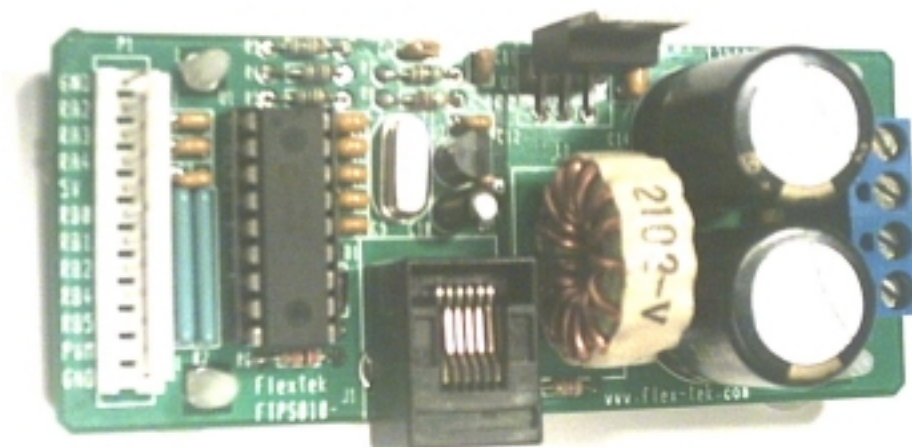


Figure 1. 8-Buck Converter Assembled PCB Photo

Operation

The buck converter in Figure 2 has a microcontroller with ADC (Analog to Digital Converter) to measure output voltage and PWM (Pulse Width Modulator) to adjust duty cycle of the half-bridge power stage. The control algorithm that calculates PWM drive to obtain the desired ADC voltage is PID (Proportional-Integral-Differential). Sample waveforms are shown in Figure 3 to illustrate basic operation.

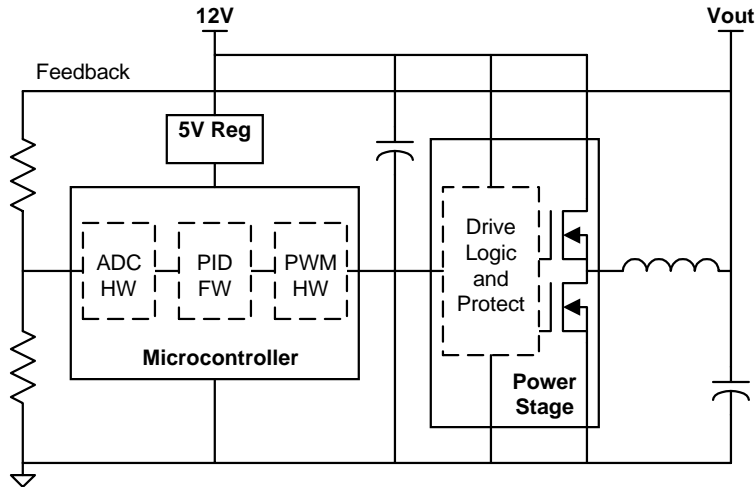


Figure 2. 8-Buck Converter Block Diagram

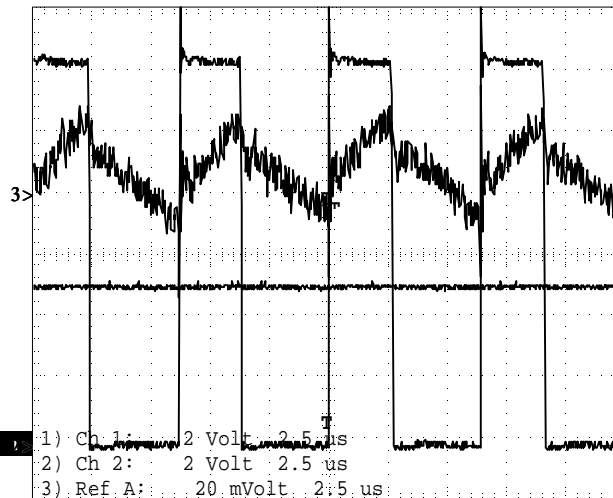


Figure 3. Waveforms show Output Voltage is Average of Switching Power

- 1) Switching power stage (2V/div, 2.5uS/div)
- 2) Filtered output voltage (2V/div, 2.5uS/div)
- 3) Output voltage ripple (20mV/div, 2.5uS/div)

Operational parameters are summarized in Figure 4. Figure 5 shows start-up voltage and Figure 6 illustrates benefit of closed-loop control to stepped load. Converter output voltage is 5.0V when digital input pin ADJ (PIC RB0) is high (open) and 3.3V when ADJ is low (grounded). The converter is enabled when D1 (RB1) is high. STA (RA2) output is high while enabled if no faults are detected.

Ratings	10V-14Vin, 1V-11Vout @ 7.3A
Size	1.5in W x 3.6in L x 0.9in H, 2 oz. Wt.
Efficiency	92% at 5V/7A Output
Switching	156KHz, 7 bit resolution (94mVout)
Update	25.6 μ S (PWM adjusted every 4th cycle)
Process	38.4 μ S (19.2 μ S ADC + 19.2 μ S PID)
ADC	10 bit resolution (11mVout), 19.2 μ S conversion
Ripple	12mVrms (switch + quantization)
Transient	Δ Vpk = 60mV/A, 200 μ S Recovery

Figure 4. Converter Summary Table

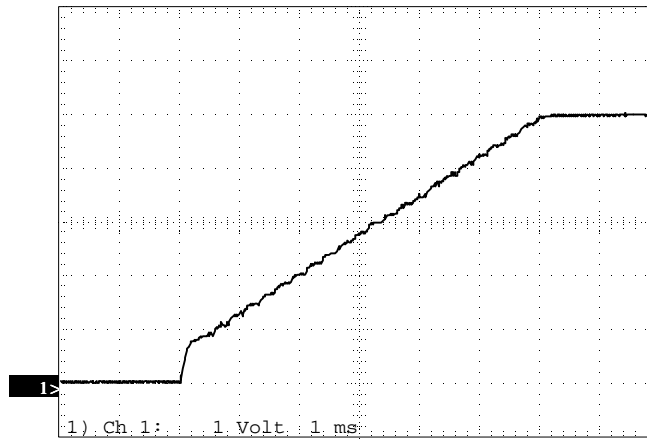


Figure 5. Converter Soft-Start Output Voltage

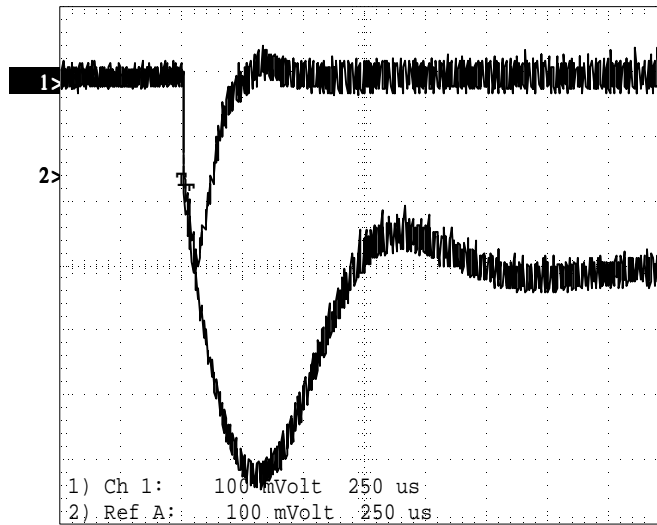


Figure 6. Open and Closed Loop Response of Converter to Step Load

Hardware

Assemble PCB of Figure 7 with components in Figure 8. Low number of through-hole parts facilitates process. Save time by registering at www.digi-key.com and uploading file 8BUCKPL.TXT in CSV/TAB format. Expect single order of parts to cost about \$34 plus shipping and tax.

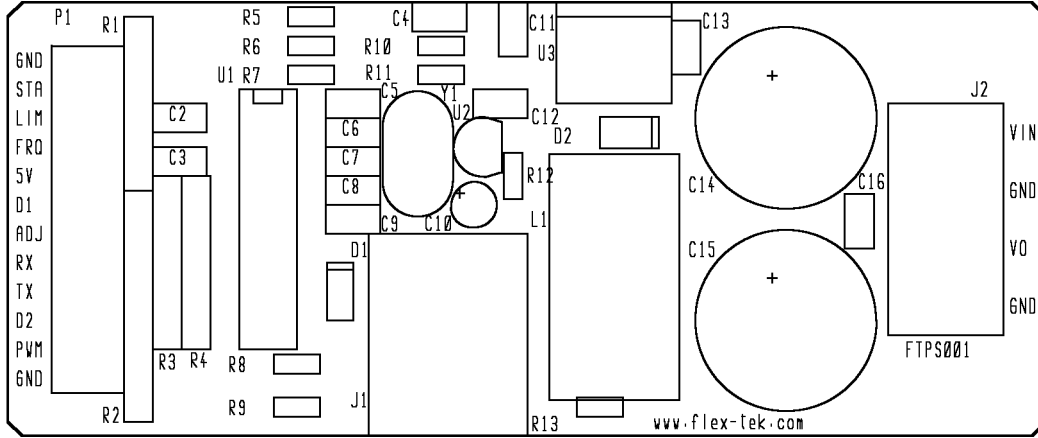


Figure 7. 8BUCK Converter PCB Parts Placement

FN	Qty	MANUFACT	PART NO	DESCRIPTION	REF DES
1	1	FLEXTEK	FTPS001	PCB	PCB1
2	1	ASSMAN	A18-LC-TT	SOCKET, 18PIN DIP	SK1
3	1	MICROCHIP	PIC16F818-I/P	IC, PIC MICRO 18PIN DIP	U1
4	1	NAT SEMI	LP2950CZ-5.0	IC, 5V VOLT REG TO-92	U2
5	1	INFINEON	TDA21201-S7	IC, HALF BRIDGE, TO220-7	U3
6	1	FAIRCHILD	1N5232B	DIODE, 5.6V ZENER, 0.5W	D1
7	1	DIODES INC	1N4744A	DIODE, 15V ZENER, 1W	D2
8	1	AMP	1-640456-2	HEADER, 12PIN, MTA 0.1"	P1
9	1	MOLEX	95001-2661	CONNECTOR, 6PIN. MOD JACK	J1
10	1	ON SHORE	ED120/4DS	CONNECTOR, 4PIN, TERM BLK	J2
11	1	ECS	ECS-200-20-4	CRYSTAL, 20MHZ, 20PF PAR	Y1
12	1	JW MILLER	2101-V	INDUCTOR, 10UH, 10A	L1
13	3	KEMET	C315C222K1R5CA	CAPACITOR, 0.0022U, CER	C2,C3,C5
14	5	KEMET	C315C104M5U5CA	CAPACITOR, 0.1U, CER	C4,C6,C9,C11,C12
15	2	KEMET	C315C220J2G5CA	CAPACITOR, 22P, CER	C7,C8
16	1	PANASONIC	ECE-A0JKA470	CAPACITOR, 47U, ALUM	C10
17	2	BC COMP	K105Z20Y5VE5TL2	CAPACITOR, 1U, CERAMIC	C13,C16
18	2	PANASONIC	EEU-FC1C222S	CAPACITOR, 2200U, ALUM	C14,C15
19	3	CTS	77063121	RESISTOR, 120R, NET (3) ISO	R1,R3,R4
20	1	CTS	77081203	RESISTOR, 20K, NET (7) BUS	R2
21	3	PANASONIC	ERO-S2PHF1001	RESISTOR, 1.00K, 1%, 1/8W	R5,R6,R7
22	2	PANASONIC	ERO-S2PHF2002	RESISTOR, 20.0K, 1%, 1/8W	R8,R9
23	1	PANASONIC	ERO-S2PHF1002	RESISTOR, 1.50K, 1%, 1/8W	R10
24	1	PANASONIC	ERO-S2PHF1003	RESISTOR, 3.90K, 1%, 1/8W	R11
25	10	YAGEO	CFR-12JB-4R7	RESISTOR, 4.7R, 5%, 1/8W	R12,R13
NOTES: REF DES C1 NOT USED					

Figure 8. 8-BUCK Converter Parts List

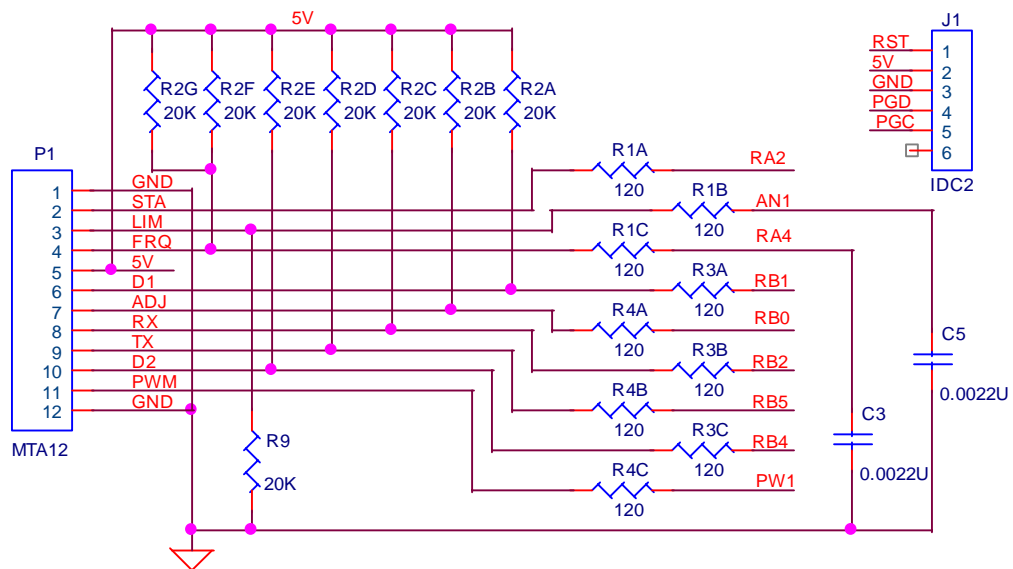
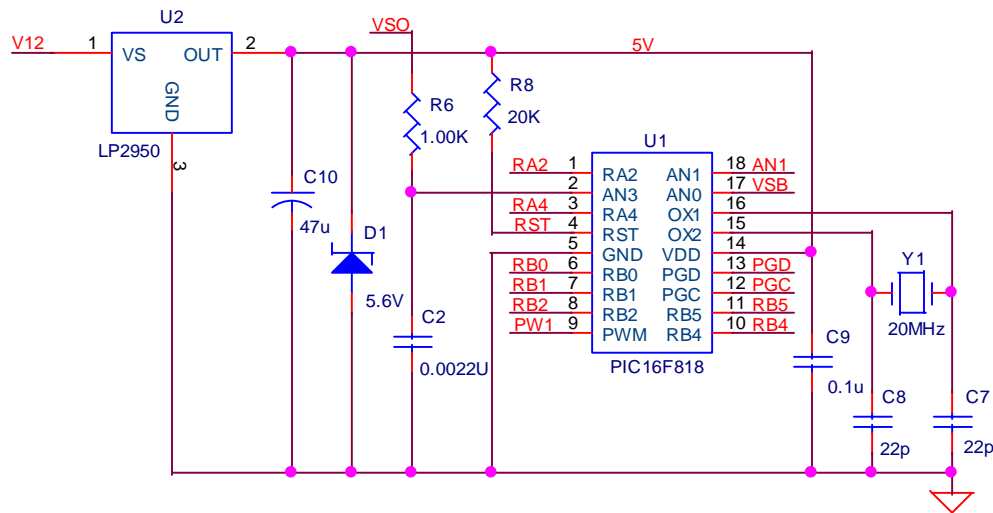
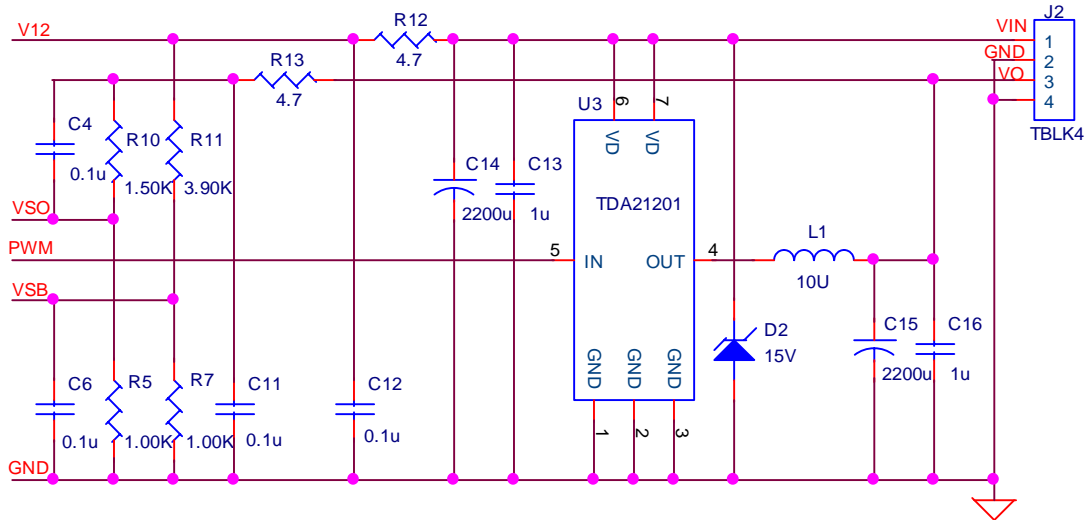


Figure 9. 8-Buck Converter Schematic

Firmware

Programmed PIC Micro in kit for initial operation prior to customization shown in Figure 10. Firmware follows timing in Figure 11 and flow in Figure 12. Source code contains comments and explanations essential for complete understanding.

Flextek retains ownership of firmware and prohibits distribution of source code, but allows compiled machine code to be freely distributed in PIC Micro chips. Firmware is not covered by product support or warranty.



Visit www.microchip.com for programming hardware, software, and documentation if required.

Figure 10. PIC Micro Development System with In-Circuit Debugger 2

Main Loop (<256 Instructions)
 Voltage Setting (5V or 3.3V)
 Soft Start (0.75V/mS),
 Status and Shutdown (0.1Sec Delay)
 Polled Timer (256uS) Loop
 (Equivalent to 5MHz PIC since operates 25% of time at 20MHz)
Interrupt Code (<96 Instructions) Every 4TH PWM (25.6uS)
 PID Control of Output Voltage
 ADC Triggered in PID Code
 (Integration every other cycle to increase throughput)

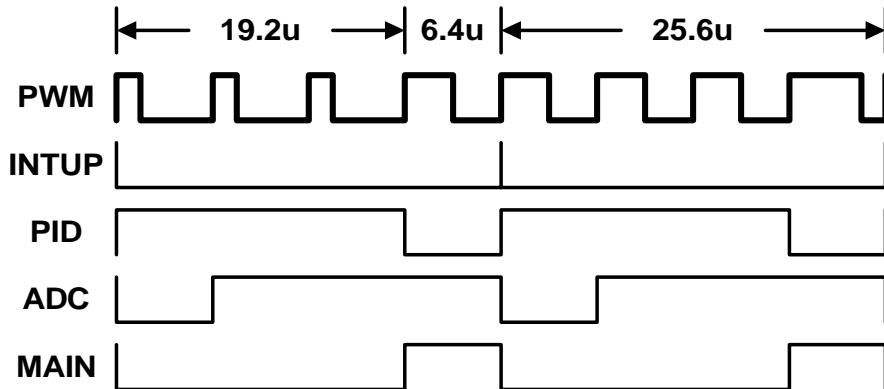


Figure 11. Micro Timing Chart

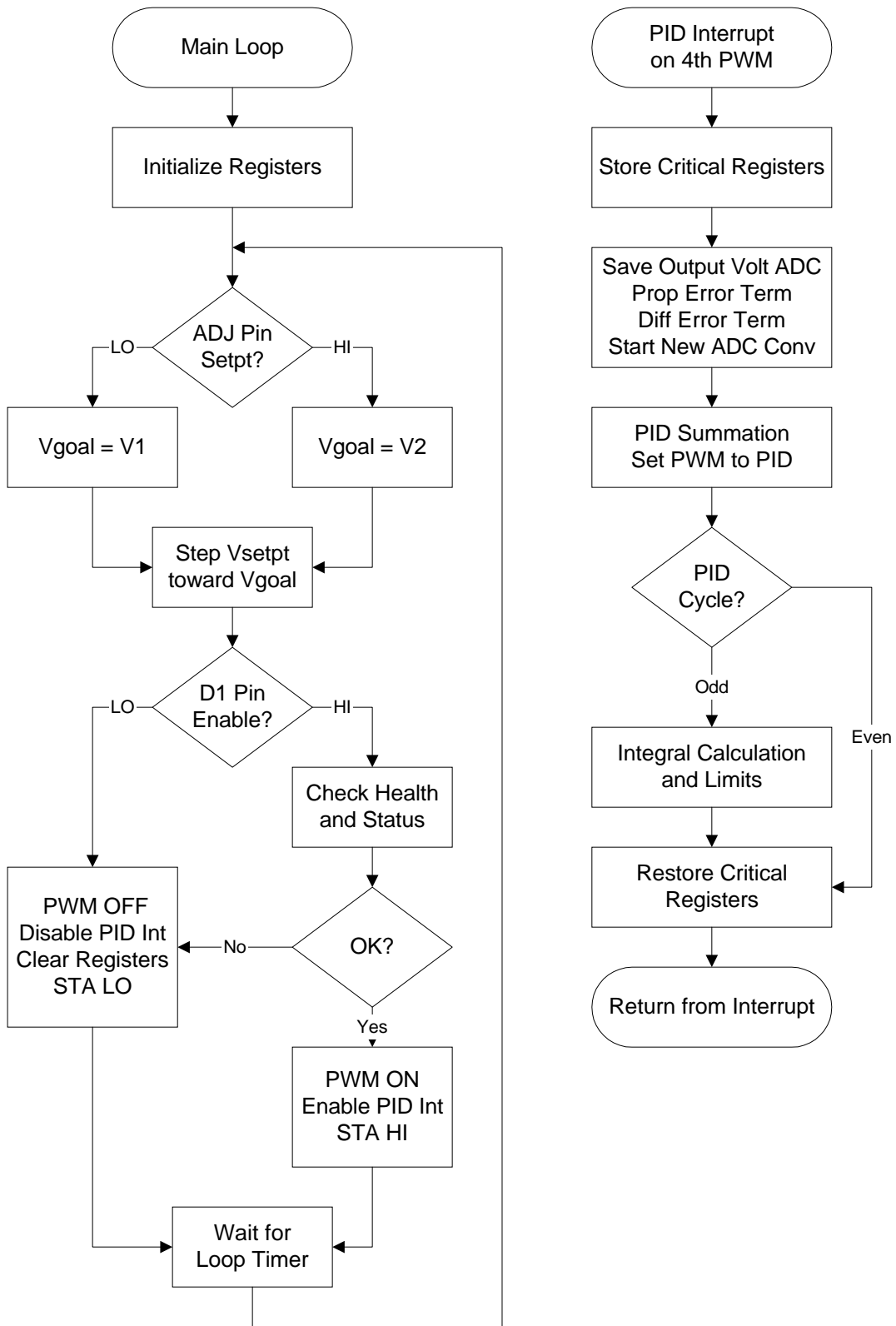


Figure 12. 8-Buck Converter Firmware Flowchart

SPICE

Creating an analog equivalent of a power converter with digital control is done by averaging, which is valid because switching frequency and PID updates are much faster than LC output filter response. The power stage and control algorithm with associated delays are simulated with op-amps and RC networks. The true value of this model is the intuitive understanding that it provides and the ability to leverage existing knowledge from traditional power converters.

PID control is calculated in firmware by the micro every update interval as follows:

$V_{err} = V_{ref} - V_{adc}$; Error = Setpoint - Measured
$V_{errDiff} = V_{err} - V_{errLast}$; Differential error between samples
$V_{errLast} = V_{err}$; Save current error for next differential calculation
$P = K_P \cdot V_{err}$; K_P = Proportional Gain = 4 in 8-Buck code
$I = I + K_I \cdot V_{err}$; K_I = Integral Gain = 0.25 in 8-Buck code
$D = K_D \cdot V_{errDiff}$; K_D = Differential Gain = 4 in 8-Buck code
$PWM = PID = P + I + D$; Make PWM output adjustment

PID firmware is simulated in the SPICE circuit by op-amps with the following RC components:

Select $R_{in} = 10K$
 $R_{prop} = K_P \cdot R_{in} = 4 \cdot 10K = 40K$
 $C_{int} = T_{update} / (K_I \cdot R_{in}) = 25.6\mu / (0.25 \cdot 10K) \approx 0.01\mu$
 $C_{diff} = K_D \cdot T_{update} / R_{prop} = 4 \cdot 25.6\mu / 40K \approx 0.0025\mu$

T_{update} is the 25.6 μ S update interval of the micro, whose associated delay is simulated by R_{update} and C_{update} . The processing delay is the sum of the ADC conversion time (19.2 μ S) and the PID calculation

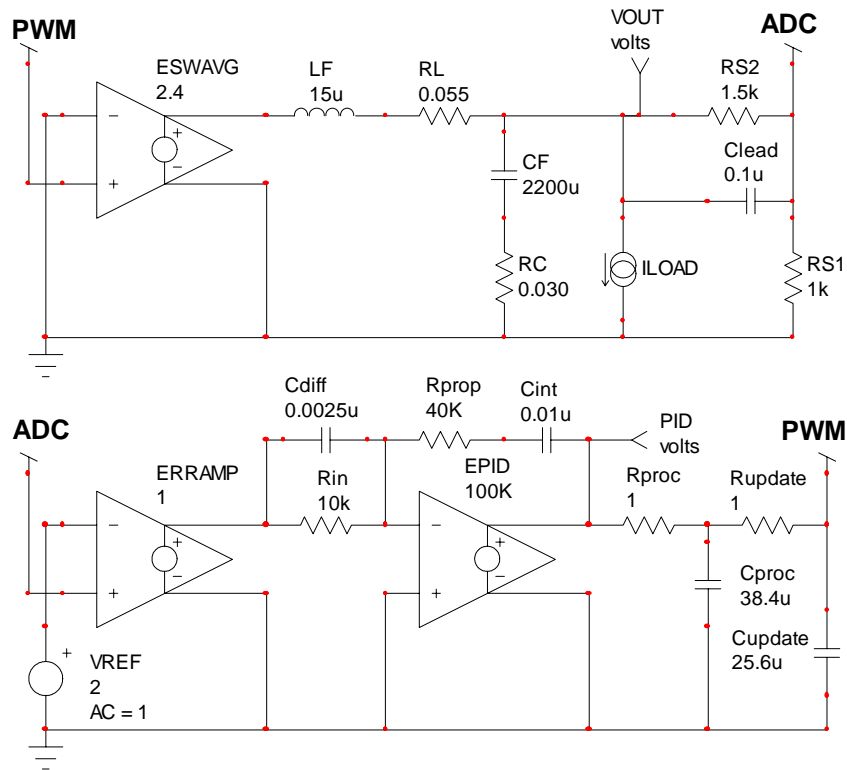


Figure 13. SPICE Equivalent of Switching Converter with Digital Control

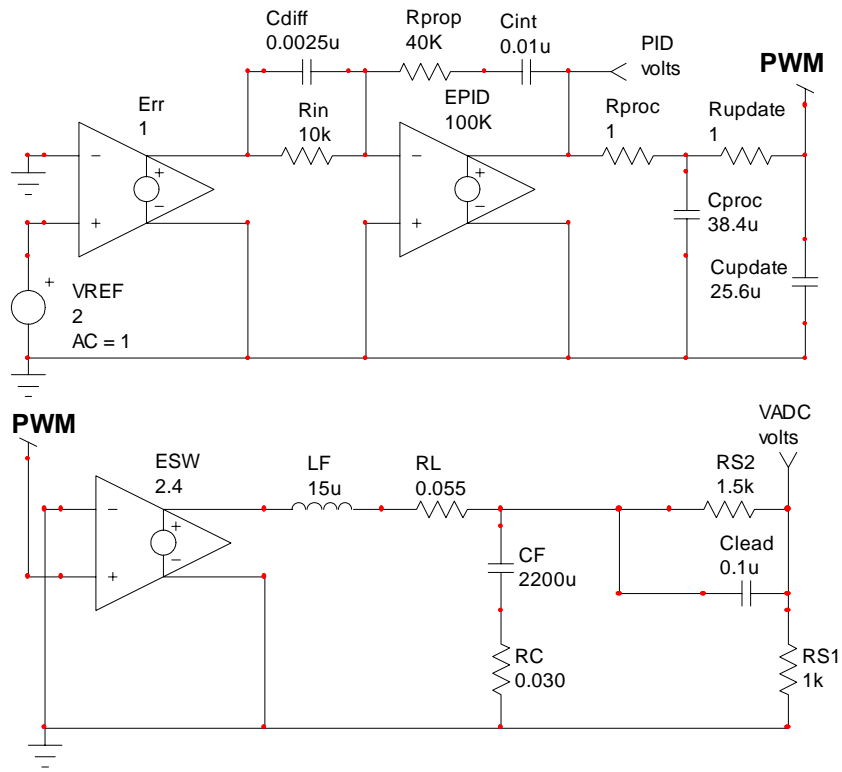


Figure 14. SPICE Circuit for Loop Gain Measurement

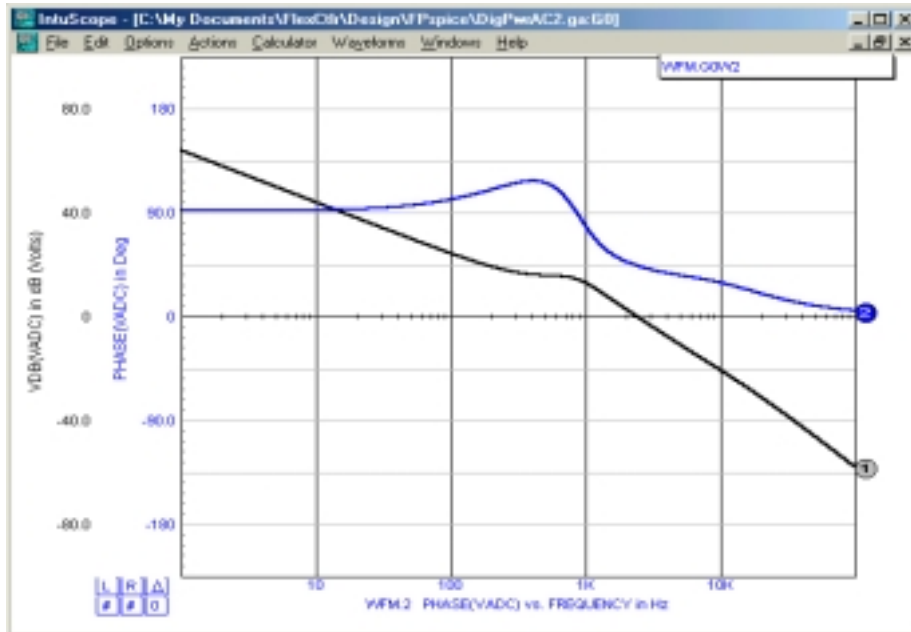


Figure 15. Loop Gain Shows 2.4KHz Bandwidth and 45° Phase Margin

Lessons

Understanding and knowledge enable designers to make effective trades and accelerate development. Guidelines help decide if the custom features of a digital converter are justified or if analog is still the best option. Use this kit for further development by upgrading to PIC16F88 for UART and comparators. Send ideas and feedback to Flextek to benefit customers and advance digital power control

Power Stage
Current limit, thermal shutdown, and under-voltage lockout protection
Tight switching path layout with power ground plane
Close charge storage capacitance and twisted power lines
Micro Hardware
Bypass capacitors and crystal close to micro pins with signal ground plane
Current limit resistors on pins to connectors
Pull-up or pull-down resistors on enable pins
Clamp VDD voltage for transients and polarity reversal
Filters on critical inputs with shielded wires
Split signal ground plane from power ground plane
Micro Firmware
Real-time operating system with multi-tasking and prioritized interrupts
Synchronize ADC sampling to PWM
Smooth transitions and operational limits
Digital filters and safeguards
Limit external interrupt rate
Prevent register overflow and underflow
Watchdog timer and brownout detection

Figure 16. Checklist for Robust Digital Power Control

Guideline 1: Critical Frequency
$f(\text{critical}) = 1 / [T_{\text{process}} + T_{\text{update}}] = 1 / [(T_{\text{adc}} + T_{\text{pid}}) + T_{\text{update}}]$
8-Buck Example: $1 / [(19.2\mu\text{s} + 19.2\mu\text{s}) + 25.6\mu\text{s}] = 15.6\text{KHz}$ limit $\ll 156\text{KHz}$ switching
Comment: Converter performance is limited by digital delays rather than switching frequency.
Guideline 2: Control Bandwidth
$f(\text{control}) < f(\text{critical}) / 4$, (Factor of 4 is limit, 10 is common, 6.3 is goal)
8-Buck Example: $15.6\text{KHz} / 6.3 = 2.5\text{KHz}$, (close to 2.4KHz simulation result)
Comment: Control loop bandwidth is bound by critical frequency.
Guideline 3: LC Filter
$LC^{1/2} > 2 / f(\text{critical}) = 2 / 15.6\text{KHz} = 128\mu\text{s}$
8-Buck Example: $[12\mu\text{H} \cdot 2200\mu\text{F}]^{1/2} = 162\mu\text{s} > 128\mu\text{s}$ (satisfied in design)
Comment: Contain LC filter resonance within loop bandwidth
Guideline 4: PWM Frequency
$f(\text{PWM}) < [f(\text{CLK}) / 2^{\text{Res}(\text{ADC})}] \cdot [LC^{1/2} / T_{\text{update}}] \cdot [V_{\text{meas}} / V_{\text{in}}]$
8-Buck Example:
$f(\text{CLK}) / 2^{\text{Res}(\text{ADC})} = 20\text{M} / 2^{10} = 19.5\text{K}$, (PWM frequency to match 10-bit ADC resolution)
$LC^{1/2} / T_{\text{update}} = 162\mu / 25.6\mu = 6.3$, (PWM adjustments within filter time constant)
$V_{\text{meas}} / V_{\text{in}} = [5 \cdot (1\text{K} + 1.5\text{K}) / 1\text{K}] / 12 = 1.04$, (Voltage ratio measurable by ADC)
$f(\text{PWM}) < 19.5\text{K} \cdot 6.3 \cdot 1.04 = 128\text{KHz}$, (Rounded up to 156KHz in design)
Comment: Maximum PWM frequency with control resolution equal to ADC.

Figure 17. Guidelines for Digital Power Control Optimization

NOTE: Refer to attached articles for complete explanations.